PERIYAR CENTENARY POLYTECHNIC COLLEGE

PERIYAR NAGAR – VALLAM – THANJAVUR – 613 403

(AUTONOMOUS INSTITUTION)

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS
ECC/16/00

SEMESTER SYSTEM
C– SCHEME

CONTENTS

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PERIYAR CENTENARY POLYTECHNIC COLLEGE

Periyar Nagar, Vallam – 613 403, Thanjavur

AUTONOMOUS INSTITUTION

VISI

Periyar Centenary Polytechnic College aspires to be recognized as one of the leaders in imparting quality technical education and strives to prepare rural students with excellent technical and life skills for the benefit of the stakeholders and society at large.

MISS

M1: To impart quality technical education to the students and equip them with knowledge, skills and attitudes that will lead to successful employment in industry/business, entrepreneurship and higher education.

M2: To provide conducive learning environment and adopt well structured teaching – learning practices to make the students technically competent.

M3: To strengthen the collaboration with industry and community for career development, placement and extension services.

M4: To develop the personality of the students and identify themselves as good individuals, professionals and responsible citizens with ethical values.

M5: To inculcate lifelong learning skills to face challenges with innovations.

PROGRAM OUTCOMES (PO

1. **Basic and Discipline specific knowledge:** Apply knowledge of basic mathematics, science and engineering fundamentals and engineering specialization to solve the engineering problems.
2. **Problem analysis:** Identify and analyse well-defined engineering problems using codified standard methods.
3. **Design/ development of solutions:** Design solutions for well-defined technical problems and assist with the design of systems components or processes to meet specified needs.
4. **Engineering Tools, Experimentation and Testing:** Apply modern engineering tools and appropriate technique to conduct standard tests and measurements.
5. **Engineering practices for society, sustainability and environment:** Apply appropriate technology in context of society, sustainability, environment and ethical practices.
6. **Project Management:** Use engineering management principles individually, as a team member or a leader to manage projects and effectively communicate about well-defined engineering activities.
7. **Life-long learning:** Ability to analyze individual needs and engage in updating in the context of technological changes.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

Create excellent diploma engineers capable of facing the contemporary and future challenges in the field of Electronics and Communication Engineering through students centred teaching learning practices with social responsibility.

MISSIO

M1: To impart quality education and training with competitive curriculum and prepare the students to excel in professional career.

M2: To provide a creative environment and equip the students with technical skills and knowledge through well structured teaching - learning process and to achieve academic excellence.

M3: To strengthen the soft skills, especially of rural students through co-curricular and extracurricular activities.

M4: To create awareness and thirst for lifelong learning through interactions with outside world regarding contemporary issues, technological trends and entrepreneurship.

PROGRAMME EDUCATIONAL OBJECTIVES

PEO1: Our Diploma graduates will have the ability to work in industry, institute and as an entrepreneur in Electronics and Communication Engineering field , pursue higher education and develop independent and lifelong learning skills for continuous professional development.

PEO2: Our Diploma graduates will be able to demonstrate technical competence in their chosen field of employment by identifying, analysing and providing engineering solutions using current techniques and tools.

PEO3: Our Diploma graduates will be able to communicate effectively and practice professional ethics and social responsibility in their career.

PROGRAMME SPECIFIC OUTCOMES

PSO1: Understand the fundamental concepts and techniques of Electronics and communication Engineering to design and develop the Electronics, Digital, Microcontroller and communication systems.

PSO2: Apply the technical knowledge and skills in VLSI design, embedded systems and advanced communication systems using appropriate tools.

PSO3: Analyze and develop relevant solutions using domain knowledge with respect to design and analysis using hardware and software tools.

OUTCOME BASED EDUCATION(OBE)

Our institution is practicing Outcome Based Education(OBE) which is a student centered instruction model that focuses on measuring student performance through outcomes. Outcomes include knowledge, skills and attitudes.

In the OBE model, the required knowledge and skill sets for a particular diploma programme is predetermined and the students are evaluated for all the required parameters (Outcomes) during the course of the program.

The OBE model measures the progress of the graduate in four parameters, which are

- Program Educational Objectives (PEO)
- Program Specific Outcomes (PSO)
- Program Outcomes (PO)
- Course Outcomes (CO)

Program Educational Objectives (PEOs) are broad statements that describe the career and professional accomplishments that the program is preparing the graduates to achieve. PEO's are measured 4-5 years after graduation.

Program Specific Outcomes (PSOs) are the statements that describe what the graduates of specific engineering program should be able to do.

Program Outcomes (POs) are narrower statements that describe what students are expected to know and be able to do by the time of graduation.

Course Outcomes(COs) are the measurable parameters which evaluates each students performance for each course that the student undertakes in every semester. The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. According to revised Bloom's taxonomy, the levels in cognitive domain are as follows:

Level	Descriptor	Level of attainment
1	Remembering	Recalling from memory of previously learned material
2	Understanding	Explaining ideas or concepts
3	Applying	Using information in another familiar situation
4	Analyzing	Breaking information into part to explore Understandings and relationships
5	Evaluating	Justifying a decision or course of action
6	Creating	Generating new ideas, products or new ways of Viewing things.

DIPLOMA COURSES IN ENGINEERING/TECHNOLOGY
(Implemented from 2015-2016)
C SCHEME
RULES AND REGULATIONS

1. Description of the course

a) Full Time (3 years)

The course for the full time Diploma in Engineering shall extend over a period of three academic years, consisting of 6 semesters* and the first year is common to all Engineering branches.

b) Sandwich (3 $^1/_2$ years)

The course for the Diploma in Engineering (sandwich) shall extend over a period of three and half academic years consisting of 7 semesters *and the First year is common to all Engineering Branches. The subjects of three years full time diploma course being regrouped for academic convenience.

During 4th and 7th semester the students undergo industrial training for six months. Industrial training examination will be conducted after completion of every 6 months of industrial training.

* Each semester will have 15 weeks duration of studies with 35 hours per week for all diploma courses.

2. Conditions for Admission

Condition for admission to the diploma course shall be required to have passed in the S.S.L.C Examination of the Board of Secondary Education, Tamil Nadu.

(or)

The Anglo Indian High School Examination with Eligibility for Higher Secondary Course in Tamil Nadu.

(or)

The Matriculation Examination of Tamil Nadu.

(or)

Any other examinations recognized as equivalent to the above by the board of Secondary Education, Tamil Nadu.

Note: In addition at the time of admission the candidate will have to satisfy certain minimum requirements, which may be prescribed from time to time.

3. Admission to Second year (Lateral Entry)

A pass in HSC [(Academic) or (Vocational)] course mentioned in the Higher Secondary Schools in Tamil Nadu Affiliated to the Tamil Nadu Higher Secondary board with eligibility for university Courses of study or equivalent examination, & Should have studied the following subjects.

Sl.No	Course	H.Sc Academic	H.Sc Vocational	
			Subjects studied	
		Subjects studied	Related subjects	Vocational subjects
1	All the	Maths, Physics &	Maths/Physics/	Related vocational

	Regular and Sandwich Diploma Courses	Chemistry	Chemistry	subjects Theory & Practical
2	Diploma in Modern Office Practice	English & Accountancy English & Elements of Economics English & Elements of Commerce	English & Accountancy, English & Elements of Economics, English & Management Principles & Techniques, English & Typewriting	Accountancy & Auditing Banking, Business Management , Co-operative Management, International Trade, Marketing & Salesmanship, Insurance & Material Management, Office Secretaryship.

- For the Diploma courses related with Engineering /Technology, the related/equivalent subjects prescribed along with Practicals may also be taken for arriving the eligibility.
- Branch will be allotted according to merit through counselling by the respective Principal as per communal reservation.
- For Admission to the Modern Office Practice Diploma course the candidates studied the related subjects will be given first preference.
- Candidates who have studied Commerce Subjects are not eligible for Engineering Diploma Course.

4. Readmission of Candidates

A student who had discontinued his/her studies in the middle of a semester or who had not appeared for Autonomous Examination of current semester of study, can apply and get readmission in the same semester in the following subsequent academic years if he/she desires to complete the course and satisfies the following conditions:

The candidate should not have exhausted the total period of study (given below) permitted to complete the course.

Full time(Regular) - 6 years

Full time (Sandwich) - 6 ½ years

Full time(Lateral Entry) - 5 years

He/She, on readmission, should be able to complete his/her full course of study within the above stipulated total period. A candidate who had discontinued his/her studies continuously or in spells for more than 3 years shall not be recommended for readmission.

Readmissions are not permissible in first year (I semester) for regular students and in third semester for lateral entry students, who have not written any Autonomous Examinations, before their discontinuance of study. They have to forego their candidature and seek admission again fresh.

5. Age Limit

No Age Limit

6. Procedure for completing the Diploma Course

A candidate will be permitted to appear for the Examination only if, he/she secures 80% of attendance.

- A student having shortage of attendance in a semester should repeat the same semester in the next academic year. Similarly, a student who had not attended at least a single paper(theory or practical) of a particular semester examination, cannot continue his/her studies in the next semester, even if he / she had enough attendance in that semester with usual conditions.

- The candidate on completion of studies in each semester should necessarily register himself / herself for the examinations of all the subjects of the semester as well as for all arrear subjects of all the previous semester and shall appear for the Autonomous Examinations.

7. **Reasons for disqualifying a student from appearing Autonomous Examinations**

- A student who had failed to acquire the minimum required percentage of attendance during a semester of study or discontinued his/her studies in the middle of a semester and who had not paid the examination fee in time shall not be permitted to appear for the Autonomous Examination
- A Student who had paid the examination fee in time, but do not have enough attendance in the course of study, shall not be permitted to appear for the Autonomous Examination however, will be permitted to write the supplementary examinations of previous semesters.

8. Eligibility for the Award of Diploma

No candidate shall be eligible for the Diploma unless he/she has undergone the prescribed course of study for a period of not less than 3 academic years in any institution affiliated to the State Board of Technical Education and Training, Tamil Nadu, when joined in first year and two years if joined under Lateral Entry scheme in the second year and passed the prescribed examination.

The minimum and maximum period for completion of Diploma Course are as given below

Diploma Course	Minimum period	Maximum Period
Full time	3 years	6 years
Full time (lateral Entry)	2 years	5 years
Sandwich	3 $^{1}/_{2}$ years	6 ½ years

9. Subjects of study and Curriculum outline:

The subjects of study shall be in accordance with the syllabus prescribed from time to time, both in theory and practical. The Curriculum outline is given in Annexure – I

10. Examinations

Autonomous Examinations in all subjects of all the semesters under the scheme of examinations will be conducted at the end of each semester.

The Internal assessment marks for all the subjects will be awarded on the basis of continuous internal assessment earned during the semester concerned. For each subject 25 marks are allotted for Internal Assessment Marks and 75 marks are allotted for Autonomous Examination.

11. Continuous Internal Assessment

A. Theory Subjects - For II & III year

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks
	Total	**-**	**25 Marks**

i) Subject Attendance **5 Marks**

(Award of marks for subject attendance to each subject Theory/Practical will be as per the range given below)

80%	-	83%	1 Mark
84%	-	87%	2 Marks
88%	-	91%	3 Marks
92%	-	95 %	4 Marks
96%	-	100%	5 Marks

ii) Test **10 Marks**

2 Tests each of 2 hours duration for a total of 50 marks are to be conducted. Out of which the best one will be taken and the marks to be reduced to: **5 Marks**

The test – III is to be the Model Test covering all the five units and the marks so obtained will be reduced to: **5 Marks**

Total **10 Marks**

Test	Units	When to conduct	Marks	Duration
Test – I	Unit I & II	End of 6th week	50	2 hrs
Test – II	Unit III & IV	End of 12th week	50	2 hrs
Test – III	**Model Examination – Compulsory** Covering all the 5 units (Autonomous Examination – question paper pattern)	End of 15th Week	75	3 hrs

Question paper pattern for the periodical Test (Test – I & Test – II)

With no Choice:

Part A	4 Questions x 2 Marks	:	08 marks
Part B	4 Questions x 3 marks	:	12 marks
Part C	3 Questions x 10 marks	:	30 marks
	Total :		**50 marks**

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iii) Assignment **5 marks**

For each subject three assignments are to be given each for 20 marks and the average marks scored should be reduced for 5 marks.

Assignment 1: Written notes in relevant topics from the subjects.

Assignment 2: Science/Technical projects – To acquire practical knowledge.

Assignment 3: Objective type online test-to understand the principles and thereby gain in-depth knowledge about the subject.

iv) Seminar **5 marks**

For seminar the total seminar 15 hours (15 weeks x 1 hour) should be distributed equally to total theory subject per semester(i.e. 15 hours divided by 3/4 subject). A topic from subject or current scenario is given to students. During the seminar hour students have to present the paper and submit seminar material to the respective staff member, who is handling the subject. It should be preserved for 2 Semesters and produced to the flying squad and the inspection team at the time of inspection/verification.

All Test papers, Assignments and Seminar Materials after getting the signature with date from the students must be kept in the safe custody in the Department for verification and audit. It should be preserved for 2 semesters and produced to the flying squad and the inspection team at the time of inspection/ verification.

For I Year General Engineering

Theory Subjects

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	10 Marks

	Total	**-**	**25 Marks**
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i) Subject Attendance **5 Marks**

(Award of marks for subject attendance to each subject Theory/Practical will be as per the range given below)

80%	-	83%	1 Mark
84%	-	87%	2 Marks
88%	-	91%	3 Marks
92%	-	95 %	4 Marks
96%	-	100%	5 Marks

ii) Test **10 Marks**

2 Tests each of 2 hours duration for a total of 50 marks are to be conducted. Out of which the best one will be taken and the marks to be reduced to: **5 Marks**

The test – III is to be the Model Test covering all the five units

and the marks so obtained will be reduced to: **5 Marks**

Total **10 Marks**

Test	Units	When to conduct	Marks	Duration
Test – I	Unit I & II	End of 6th week	50	2 hrs
Test – II	Unit III & IV	End of 12th week	50	2 hrs
Test – III	**Model Examination – Compulsory** Covering all the 5 units (Autonomous Examination – question paper pattern)	End of 15th Week	75	3 hrs

Question paper pattern for the periodical Test (Test – I & Test – II)

With no Choice:

Part A	5 Questions x 1 Mark	:	05 marks
Part B	10 Questions x 2 marks	:	20 marks
Part C	5 Questions x 5 marks	:	25 marks
	Total : 50 marks		

iii) Assignment **10 marks**

For each subject, three assignments are to be given each for 20 marks and the average marks scored should be reduced for 10 marks.

Assignment 1: Written notes in relevant topics from the subjects.

Assignment 2: Science/Technical projects – To acquire practical knowledge.

Assignment 3: Objective type online test-to understand the principles and thereby gain in-depth knowledge about the subject.

All Test papers and Assignments after getting the signature with date from the students must be kept in the safe custody in the Department for verification and audit. It should be preserved for 2 semesters and produced to the flying squad and the inspection team at the time of inspection/ verification.

B. Practical Subjects

I, II and III year

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

a) Attendance : 5 marks – (Award of marks same as theory subjects)

b) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

c) Record writing : 10 marks

Total **25 marks**

- All the Experiments/Exercises indicated in the syllabus should be completed and the same to be given for final Autonomous Examinations.
- The Record for every completed exercise should be submitted in the subsequent Practical classes and marks should be awarded for 20 for each exercise as per the above allocation.
- At the end of the Semester, the average marks of all the exercise should be calculated for 20 marks and the marks awarded for attendance is to be added to arrive at the Internal Assessment Mark for Practical.(20+5=25 Marks)
- The students have to submit the duly signed bonafide record note book/file during the Practical Autonomous Examinations.
- All the marks awarded for Assignments, Tests, Seminars and Attendance should be entered in the Personal Log Book of the staff, who is handling the subject. This is applicable to both Theory and Practical Subjects.

12. Life and Employability skills Practical

The Life and Employability skills Practical with more emphasis is being introduced in IV Semester for Circuit Branches and in III Semester for other branches of Engineering. Much Stress is given to increase the employability of students.

Internal Assessment Marks **- 25 Marks**

13. Project Work

The Students of all the Diploma courses have to do a Project Work as part of the Curriculum and in Partial fulfillment for the award of Diploma by the State Board of Technical Education and Training, Tamil Nadu. In order to encourage students to do worthwhile and innovative projects, every year prizes are awarded for the best three projects i.e. institution wise, region wise and state wise. **The Project work must be reviewed twice in the same semester.**

a) Internal Assessment Mark for Project Work & Viva Voce

Project Review I	:	10 Marks
Project Review II	:	10 marks
Attendance	:	05 marks (Award of marks same as theory subject pattern)
Total	**:**	**25 marks**

Proper record to be maintained for the two project reviews, and it should be preserved for 2 semesters and produced to the flying squad and the inspection team at the time of inspection/ verification.

b) Allocation of Marks for project work & Viva Voce in Autonomous Examination

i)	Viva Voce	:	30 marks
ii)	Report Preparation & Demonstration of Project	:	35 marks

Total	**: 65 marks**

iii) Written Test Mark (from 2 topics for 30 minutes duration) #

i) Environment Management 2 questions x 2 ½ marks = 5 marks
ii) Disaster Management 2 questions x 2 ½ marks = 5 marks

10 marks

(# Selection of questions should be from Question Bank, by the External Examiner, No Choice need be given to the candidates

Viva Voce	- 30 Marks
Report Preparation & Demonstration of Project	- 35 Marks
Written Test Mark	- 10 Marks
Total	**75 marks**

A neatly prepared PROJECT REPORT as per the format has to be submitted by individual student during the project Work & Viva voce Autonomous Examination.

14. Practical Training and Project Work for Architectural Assistantship (SW)

i. Practical Training

In IV and VII semesters, students should undergo the practical training under the registered architects without fail. During this period, they should have 80% of attendance. Candidates not fulfilling the above are not eligible to appear for the practical examinations. The candidates should redo the practical training in the next academic year.

The internal Assessment is based on the Monthly Report, Weekly Report, Attendance and Feedback given by the architects.

Work diary (internal Assessment) - 25 marks

Allocation of Marks

i) Monthly Report	- 10 Marks
ii) Weekly Report	- 5 Marks
iii) Attendance	- 5 Marks
iv) Feedback given by the architects	- 5 Marks
Total	**- 25 Marks**

Architect office and studio practice – I &II (IV & VII Sem)

Report writing	- 50 marks
Viva- voce	- 25 marks
Total	**- 75 marks**

ii. Project work

For the project work, to allocate internal assessment for the project work two reviews to be conducted and the average of two should be taken for the final assessment.

Average of two review marks (internal Assessment) – 25 marks

Project work & Viva Voce – Autonomous Examination

Record	-	20 marks
Drawing and presentation	-	30 marks
Model	-	15 marks
Viva-Voce	-	10 marks
Total	-	**75 marks**

A neatly prepared PROJECT REPORT as per the format has to be submitted by individual student during the project Work & Viva Voce Autonomous Examination.

15. Scheme of Examinations:

The Scheme of examination for subjects is given in **Annexure – II**

16. Criteria for Pass:

1. No candidate shall be eligible for the award of Diploma unless he/ she has undergone the prescribed course of study successfully in an institution approved by AICTE and affiliated to the State Board of Technical Education & Training, Tamil Nadu and pass all the subjects prescribed in the curriculum.
2. A candidate shall be declared to have passed the examination in a subject if he/she secures not less than 40 % in theory subjects and 50% in practical subject out of the total prescribed maximum marks including both the internal assessment and the Autonomous Examination marks put together, subject to the condition that he/she secures at least a minimum of 30 marks out of 75 marks in the Autonomous Theory Examinations and a minimum of 35 marks out of 75 marks in the Autonomous Practical Examinations.

17. Classification of successful candidates

Classification of candidates who will pass out the final examinations from April - 2018 onwards (joined in first year in 2015-2016) will be done as specified below.

First Class with Superlative Distinction:

A candidate will be declared to have passed in **First Class with Superlative Distinction** if he/she secures not less than 75% of the marks in all the subjects and passes all the semesters in the first appearance itself and passes all subjects within the stipulated period of study 3/ 3 ½ years (Full time/Sandwich) without any break in study.

First Class with Distinction:

A candidate will be declared to have passed in **First Class with Distinction** if he/she secures not less than 75% of the aggregate marks in all the semesters put together and passes all the semesters except the I and II

semester in the first appearance itself and passes all subjects within the stipulated period of study 3/3 ½ years (Full time/Sandwich) without any break in study.

First Class:

A candidate will be declared to have passed in **First Class** if he/she secures not less than 60% of the aggregate marks in all the semesters put together and passes all the subjects within the stipulated period of study 3 / 3 ½ years (Full time/Sandwich) without any break in study.

Second Class

All other successful candidates will be declared to have passed in **Second Class.**

18. Duration of a period in the class time table

The duration of each period of instruction is 1 hour and the total period of instruction hours excluding interval and Lunch break in a day should be uniformly maintained as 7 hours corresponding to 7 periods of instruction (Theory & Practical)

19. Issue of mark sheets / Diploma Certificates – Regarding with –held results

The final semester mark sheets of candidates who pass in the final semester examination, but do have arrears in the lower semester examinations will be **with-held** till they clear all the arrears.

20. Revaluation of Examination papers

- Any candidates can apply for revaluation of his / her answer script of any theory paper he/she had appeared.
- The candidates has to fill in the prescribed application form and remit fee (Rs.100/- per paper) for getting the Xerox copy of answer script within 15 days from the date of publication of results.
- The Xerox copy of the semester script will be sent to the candidate's address directly within 15 days from the date of receipt of application.
- If the candidate desires for revaluation of his/her answer script, he/she has to fill the application form enclosed with Xerox copy, pay the revaluation fee (Rs. 400/- per paper) within one week from the date of sending Xerox copy.
- The script will be revalued and the revised marks will be intimated to the candidates.
- The revaluation system is applicable for the practical subjects and project work.
- Applications received after the prescribed due dates will not be entertained.

Conclusion

The above rules and regulations can be amended, revised and altered as per the DOTE norms and Academic Board.

ANNEXURE – I

CURRICULUM OUTLINE

THIRD SEMESTER

Sl.No	Subject Code	SUBJECT	HOURS PER WEEK			
			Theory Hours	Tutorial/ Drawing	Practical Hours	Total Hours
1.	ECC 310	Electronic Devices and Circuits *	5	-	-	5
2.	ECC 320	Electrical Circuits and Instrumentation	6	-	-	6
3.	ECC 330	Programming in 'C'	5	-	-	5
4.	ECC 340	Electronic Devices and Circuits Practical*	-	-	4	4
5.	ECC 350	Electrical Circuits and Instrumentation Practical	-	-	4	4
6.	ECC 360	Programming in 'C' Practical	-	-	5	5
7.	ECC 370	Computer Application Practical for Electronics	-	-	4	4
		Library	1	-	-	1
		Seminar	1	-	-	1
		Total	18	-	17	35

* Common with EEE

FOURTH SEMESTER

Sl.No	Subject Code	SUBJECT	HOURS PER WEEK			
			Theory Hours	Tutorial/ Drawing	Practical Hours	Total Hours
1.	ECC 410	Industrial Electronics	5	-	-	5
2.	ECC 420	Communication Engineering	5	-	-	5
3.	ECC 430	Digital Electronics *	5	-	-	5
4.	ECC 440	Linear Integrated Circuits	4	-	-	4
5.	ECC 450	Industrial Electronics & Communication Engineering Practical	-	-	5	5
6.	ECC 460	Integrated Circuits Practical*	-	-	5	5
7.	ECC 470	Life and Employability Skills Practical #	-	-	4	4
		Library	1	-	-	1
		Seminar	1	-	-	1
		Total	21	-	14	35

* Common with EEE

Common for all branches

FIFTH SEMESTER

Sl.No	Subject Code	SUBJECT	HOURS PER WEEK			
			Theory Hours	Tutorial/ Drawing	Practical Hours	Total Hours
1.	ECC 510	Advanced Communication Systems	5	-	-	5
2.	ECC 520	Microcontroller *	5	-	-	5
3.	ECC 530	Very Large Scale Integration	6	-	-	6
4.	ECC 541 ECC 542 ECC 543	Elective – I 1. Digital Communication 2. Programmable Logic Controller 3. Bio Medical Instrumentation	5	-	-	5
5.	ECC 550	Advanced Communication Systems Practical	-	-	4	4
6.	ECC 560	Microcontroller Practical*	-	-	4	4
7.	ECC 570	Very Large Scale Integration Practical	-	-	4	4
		Library	1	-	-	1
		Seminar	1	-	-	1
		Total	23	-	12	35

***Common with EEE**

SIXTH SEMESTER

Sl.No	Subject Code	Subject	HOURS PER WEEK			
			Theory Hours	Tutorial/ Drawing	Practical Hours	Total Hours
1.	ECC 610	Embedded Systems	6	-	-	6
2.	ECC 620	Computer Hardware Servicing and Networking	5	-	-	5
3.	ECC 631 ECC 632 ECC 633	Elective – II 1. Television Engineering 2. Test Engineering 3. Mobile Communication	5	-	-	5
4.	ECC 640	Embedded Systems Practical	-	-	4	4
5.	ECC 650	Computer Servicing and Network Practical	-	-	4	4
6.	ECC 660	Advanced Microcontroller & Simulation Practical	-	-	4	4
7.	ECC 670	Project work	-	-	5	5
		Library	1	-		1
		Seminar	1	-		1
		Total	18	-	17	35

ANNEXURE – II

SCHEME OF THE EXAMINATION

THIRD SEMESTER

Sl. No	Subject Code	Subject	EXAMINATION MARKS			Minimum for pass	Duration of Exam Hours
			Internal assessment Marks	Auton-omous Exam marks	Total		
1.	ECC 310	Electronic Devices and Circuits	25	75	100	40	3
2.	ECC 320	Electrical Circuits and Instrumentation	25	75	100	40	3
3.	ECC 330	Programming in 'C'	25	75	100	40	3
4.	ECC 340	Electronic Devices and Circuits Practical	25	75	100	50	3
5.	ECC 350	Electrical Circuits and Instrumentation Practical	25	75	100	50	3
6.	ECC 360	Programming in 'C' Practical	25	75	100	50	3
7.	ECC 370	Computer Application Practical for Electronics	25	75	100	50	3
TOTAL			**175**	**525**	**700**		

FOURTH SEMESTER

Sl. No	Subject Code	Subject	EXAMINATION MARKS			Minimum for pass	Duration of Exam Hours
			Internal assessment Marks	Auton-omous Exam marks	Total		
1.	ECC 410	Industrial Electronics	25	75	100	40	3
2.	ECC 420	Communication Engineering	25	75	100	40	3
3.	ECC 430	Digital Electronics	25	75	100	40	3
4.	ECC 440	Linear Integrated Circuits	25	75	100	40	3
5.	ECC 450	Industrial Electronics & Communication Engineering Practical	25	75	100	50	3
6.	ECC 460	Integrated Circuits Practical	25	75	100	50	3
7.	ECC 470	Life and Employability Skills Practical	25	75	100	50	3
TOTAL			**175**	**525**	**700**		

FIFTH SEMESTER

Sl. No	Subject Code	Subject	EXAMINATION MARKS			Minimum for pass	Duration of Exam Hours
			Internal assessment Marks	Auton-omous Exam marks	Total		
1.	ECC 510	Advanced Communication Systems	25	75	100	40	3
2.	ECC 520	Microcontroller	25	75	100	40	3
3.	ECC 530	Very Large Scale Integration	25	75	100	40	3
4.	ECC 541 ECC 542 ECC 543	Elective – I 1. Digital Communication 2. Programmable Logic Controller 3. Bio Medical Instrumentation	25	75	100	40	3
5.	ECC 550	Advanced Communication Systems Practical	25	75	100	50	3
6.	ECC 560	Microcontroller Practical	25	75	100	50	3
7.	ECC 570	Very Large Scale Integration Practical	25	75	100	50	3
TOTAL			**175**	**525**	**700**		

SIXTH SEMESTER

Sl. No	Subject Code	Subject	EXAMINATION MARKS			Minimum for pass	Duration of Exam Hours
			Internal assessment Marks	Auton omous Exam marks	Total		
1.	ECC 610	Embedded Systems	25	75	100	40	3
2.	ECC 620	Computer Hardware Servicing and Networking	25	75	100	40	3
3.	ECC 631 ECC 632 ECC 633	Elective – II 1. Television Engineering 2. Test Engineering 3. Mobile Communication	25	75	100	40	3
4.	ECC 640	Embedded Systems Practical	25	75	100	50	3
5.	ECC 650	Computer Servicing and Network Practical	25	75	100	50	3
6.	ECC 660	Advanced Microcontroller & Simulation Practical	25	75	100	50	3
7.	ECC 670	Project work	25	75	100	50	3
TOTAL			**175**	**525**	**700**		

ECC 310 ELECTRONIC DEVICES AND CIRCUITS

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
			Marks			
Electronic Devices and Circuits	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**Semester End Examination**	**Total**	**Duration**
	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPIC	TIME(HRS)
I	Semiconductor and Diodes	12
II	Bipolar Junction Transistor	12
III	Transistor oscillators and FET and UJT	13
IV	SCR,DIAC,TRIAC,MOSFET and IGBT	13
V	Opto Electronic Devices and Wave shaping Circuits	13
	Revision and Test	12
TOTAL		**75**

COURSE DESCRIPTION

Every Electronics Engineer should have sound knowledge about the components used in Electronics Industry. This is vital in R&D Department for chip level troubleshooting. To meet the industrial needs, diploma holders must be taught about the most fundamental subject, Electronic Devices and Circuits. By studying this subject, they will be skilled in handling all types of electronic devices and able to apply the skill in electronics system.

OBJECTIVES:

On completion of the following units of syllabus contents, the students must be able to:

- Study the working principle of PN junction diode and transistor
- Understand the working principle of different types of rectifier
- Understand the different transistor configurations
- Differentiate various types of amplifiers
- Study the performance of special devices like UJT, FET.
- Study the performance of different transistor oscillators
- Study the performance of SCR, DIAC, and TRIAC
- Study the performance of MOSFET and IGBT
- Know the construction and working principle of optoelectronic devices
- Study the performance of Solar cell with principle and applications
- Explain the concept of Wave shaping circuits
- Study the working principle of clippers and clampers

COURSE OUTCOMES

ECC 310 ELECTRONIC DEVICES AND CIRCUITS	
After successful completion of this course, the students should be able to	
C310.1	Explain the basic concepts of Semiconductors, diodes such as P-N junction diode, Zener diode and apply the basics of diode to describe the working of rectifier circuits such as Full and half wave rectifiers.
C310.2	Interpret the operation, applications of NPN and PNP transistor, three transistor configurations , its application in amplifiers and negative feedback concepts.
C310.3	Identify the application of transistors in Oscillators and the operation of FET ,UJT and its applications.
C310.4	Illustrate the construction , operation , characteristics and applications of SCR,DIAC,TRIAC & MOSFET.
C310.5	Interpret the construction , operation , characteristics of Opto Electronic Devices and wave shaping circuits to apply in the real life applications.

ECC 310 ELECTRONICDEVICES AND CIRCUITS

UNIT -I
SEMICONDUCTOR AND DIODES **[12 HRS]**

Semiconductor - Definition, classification, intrinsic and extrinsic N type & P type - drift current &diffusion current	[2 Hrs]
Diodes – PN junction diode	[1Hr]
Forward and Reverse bias characteristics – specification	[1Hr]
Zener diode construction &working principle-characteristics	[1 Hr]
Zener break down-avalanche break down -Zener Diode as a voltage regulator applications – specifications	[1 Hr]
Rectifier – introduction-classification of rectifiers	[1Hr]
half wave rectifier-full wave Rectifier(center tapped, bridge)	[2 Hrs]
(no mathematical equations)-comparison	[1Hr]
Applications-filters-C, LC and PI filters	[2Hrs]

UNIT-II

BIPOLAR JUNCTION TRANSISTOR **[12 HRS]**

Transistor – NPN and PNP transistor – operation	[1 Hr]
Transistor as an amplifier– Transistor as a switch-Transistor biasing	[2 Hrs]
Fixed bias, Collector base bias, Self bias	[1 Hr]
CB, CE, CC Configurations – Characteristics	[1Hr]
Comparison between three configurations in terms of input impedance	[2Hrs]
Output impedance, Current gain, Voltage gain	
Classification of amplifiers	[1 Hr]
RC coupled amplifier – Emitter follower and its application	[2Hrs]
Negative feedback Concept – effect of negative feedback	[1Hr]
Types of Negative feedback connections	[1 Hr]

UNIT-III

TRANSISTOR OSCILLATORS AND FET AND UJT	**[13 HRS]**
Transistor oscillator – Classifications	[2 Hrs]
Condition for oscillations (Barkhausen criterion)	[1Hr]
General form of LC oscillator – Hartley Oscillator Colpitts Oscillator	[2Hrs]
RC Phase shift oscillator, Crystal oscillator.	[2Hrs]
Field Effect Transistor – Construction – Working principle of FET	[1Hr]
Difference between FET and BJT- Classification of FET	[1Hr]
Characteristics of FET – Applications	[1 Hr]
FET amplifier(Common source amplifier)	[1 Hr]
UniJunctionTransistor – Construction – Equivalent circuit	[1 Hr]
Operation – Characteristics – UJT as a relaxation oscillator.	[1Hr]

UNIT IV

SCR, DIAC,TRIAC & MOSFET	**[13 HRS]**
SCR -Introduction – Working VI Characteristics	[2 Hrs]
Comparison between SCR and transistor	[1Hr]
SCR as a switch, Controlled rectifier	[2Hrs]
TRIAC working principle Characteristics	[1Hr]
DIAC–characteristics - DIAC as bi-directional switch.	[2 Hrs]
MOSFET – types & characteristics of N channel MOSFET and P channel MOSFET	[2Hrs]
Characteristics of enhancement and depletion mode MOSFET	[1Hr]
MOSFET as a switch.Applications of SCR,TRIAC, DIAC and MOSFET.	[1 Hr]
IGBT Structure and Characteristics	[1Hr]

UNIT V

OPTO ELECTRONICS DEVICES AND WAVESHAPING CIRCUITS	**[13Hrs]**
Classification of opto electronic devices	[2 Hrs]
Symbols, Characteristics, working of LDR, LED, 7 segment LED and LCD	[2Hrs]
opto coupler - Photo transistor	[2 Hrs]
Clipper, Clamper Circuits and waveforms only	[1Hr]
Solar Cell - Principles -Applications.	[1Hr]
Astable, Monostable and Bi-stable Multivibrators using Transistors	[2Hrs]
Schmitt Trigger using Transistors	
Solar Cell Series and Parallel Connection of Solar Cells –Types-Application.	[1 Hr]
SMD Components-SMD Capacitor SMD Diode-SMD Resistor SMD LED	[2Hrs]
Revision and Test	**[12 Hrs]**

TEXT BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Electronic Devices and Circuits	Sallaivahanan, N.Suresh Kumar, A.Vallavaraj	Tata McGraw Publication 3rd Edition 2016
2.	Electronics Devices and circuit theory	Boyestad&Nashelsky	PHI , New Delhi 2009

REFERENCE BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Electronic Principles	Malvino	Tata McGraw Hill Publication 2010
2.	Electronics Devices & Circuits	Allen Mottershed	PHI, 2009
3.	Electronics Devices & Circuits	Jacob Millman and Halkias	Tata McGraw – Hill publication 3rd Edition 2010
4.	Optical Fiber Communication	GerdKeiser	Tata McGraw – Hill Publication 5th Edition 2013

LEARNING WEBSITES

1.https://www.electronics-tutorials.ws/

2.http://www.learnabout-electronics.org/

3.http://www.circuitstoday.com/4-great-books-to-study-basic-electronics

4.https://www.build-electronic-circuits.com/how-to-learn-electronics/

5.https://www.seeedstudio.com/blog/2017/02/24/electronic-websites/

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C310.1	**3**	**2**	**2**	**1**	**1**	**2**	**3**	**3**	**2**	**2**
C310.2	**3**	**2**	**2**	**1**	**1**	**2**	**3**	**3**	**2**	**2**
C310.3	**3**	**2**	**2**	**1**	**1**	**2**	**3**	**3**	**2**	**2**
C310.4	**3**	**2**	**2**	**1**	**1**	**2**	**3**	**3**	**2**	**2**
C310.5	**3**	**2**	**2**	**1**	**1**	**2**	**3**	**3**	**2**	**2**
C310 Total	**15**	**10**	**10**	**5**	**5**	**10**	**15**	**15**	**10**	**10**
Correlation Level	**3**	**2**	**2**	**1**	**1**	**2**	**3**	**3**	**2**	**2**

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 320 ELECTRICAL CIRCUITS AND INSTRUMENTATION

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
			Marks			
Electrical Circuits & Instrumentation	**Hrs/ Week**	**Hrs/ Semester**	**Internal Assessment**	**End Semester Examination**	**Total**	**Duration**
	6	90	25	75	100	3 Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME(HRS)
I	DC Circuits and Theorems	16
II	AC Circuits and Resonance	16
III	Transformers and Machines	16
IV	Measuring Instruments and CRO	15
V	Transducers, Sensors & Test Instruments	15
Revision and Test		12
TOTAL		90

COURSE DESCRIPTION

This subject enables the students with concepts of DC, AC circuits and fundamentals of Electrical machines .The subject also deals with concepts, principles and working of analog and digital electronic measuring instruments. The introduction of this subject will enable the students to be well exposed to a wide area of various electronic measuring instruments and a through knowledge of the fundamentals of electrical circuits.

OBJECTIVES:

- To Study Ohm's law and Kirchhoff's laws.
- To Study the circuit theorems
- To learn about series and parallel Circuits.
- To learn various terms related to AC circuits.
- To understand concept of AC circuits
- To learn about series and parallel resonance circuits.
- To Study about transformer and its working.
- To understand the working of DC machine.
- To know about Induction motors and stepper motor.
- To understand the basic measuring instruments.
- To learn about bridge circuits.
- To discuss about CRO and its types.
- To learn about transducers and its various types.
- To Study about Sensors
- To know about test instruments.

COURSE OUTCOMES

ECC 320 ELECTRICAL CIRCUITS & INSTRUMENTATION	
After successful completion of this course, the students should be able to	
C320.1	Solve D.C. circuits by using KVL and KCL ,analyze and apply network theorems for finding the solutions of D.C circuits problems.
C320.2	Analyze A.C. circuits, derive and evaluate their various circuit parameters like impedance, reactance, admittance, conductance ,Phase angle, power factor ,power and resonance circuits with resonance condition.
C320.3	Build the knowledge on construction , working principle, EMF Equation ,Losses of Transformer and analyze various D.C machines and their real life applications.
C320.4	Determine the basic definitions of measuring instruments and analyse the construction , operation , characteristics of PMMC, DC ammeter,DC voltmeter, bridges, CRO , Function Generator and their applications.
C320.5	Explain the construction ,characteristics and application of Transducers, LVDT, RVDT Load cell, Thermocouple, Thermistor, Sensors, test instruments like of DVM , Digital frequency counter and Simple PC based Data Acquisition system.

ECC 320 ELECTRICAL CIRCUITS AND INSTRUMENTATION

UNIT I

D.C. CIRCUITS AND THEOREMS **[16Hrs]**

Definition and unit for voltage, current, power, resistance, conductance [2 Hrs]

Resistivity Ohm's law – only simple problems in Ohm's law [2 Hrs]

Kirchhoff's current law and voltage law- Series circuits –parallel circuits [3 Hrs]

Series parallel circuits-Mesh Method (simple problems) [2 Hrs]

Thevenin's - Norton's theorems [3 Hrs]

Super position and Maximum power transfer theorem [2 Hrs]

Statement and Explanation (simple problems) [2 Hrs]

UNIT II

A.C. CIRCUITS AND RESONANCE **[16 Hrs]**

AC through single pure resistance, pure inductance, pure capacitance [2 Hrs]
Voltage and current relationship

and (to mention only) the equation for power and power factor in each case [2 Hrs]
(only simple problems).

Definition for impedance, reactance, admittance, conductance, impedance, [2 Hrs]
Phase angle, power factor and power.

AC circuits – Derivation for impedance and admittance, power and [2 Hrs]

Power factor in Series and Parallel R-L ,R-C ,R-L-C circuits. [3 Hrs]

Analysis of Parallel R-L circuit, R-C circuit, R-L-C circuit
(Qualitative treatment only)

Resonance

Resonance series resonance – parallel resonance - condition for resonance [2 Hrs]

Resonant frequency-Q factor - resonance curve [3 Hrs]

Bandwidth (only simple problems).

UNIT III

TRANSFORMERS AND MACHINES **[16 Hrs]**

TRANSFORMERS

Transformer – Ideal transformer -construction - working principle [2 Hrs]

EMF equation Losses in transformer-core loss, copper loss- Efficiency [2 Hrs]

Regulation OC, SC tests on transformer [2 Hrs]

List of applications (qualitative treatment only) [2 Hrs]

MACHINES

D.C. Machines - DC–Generator –Working principle - Types- Applications [2 Hrs]
DC motor- working principle - types- applications (qualitative treatment only)
Single phase induction motor- types- construction and principle of [2 Hrs]
operation of capacitor start induction motor- Applications
Stepper motor-working principle-uses(qualitative treatment only) [3Hrs]
Universal Motor (qualitative treatment only)
Difference between single phase and three phase supply.
Rating and power consumption of induction motor . [1 Hr]

UNIT IV

MEASURING INSTRUMENTS AND CRO **[15 Hrs]**

MEASURING INSTRUMENTS

Definition for Measurement, Instrument-Errors in Measurement-Calibration [2 Hrs]
Indicating instruments – Basic forces for indicating instruments-
Construction and operation Of permanent magnet moving coil Instrument [2 Hrs]
Advantages –Disadvantages of PMMC
Shunts and Multipliers -DC ammeter-DC voltmeter-voltmeter sensitivity [2 Hrs]
Bridges- Types - Wheat stone bridge -applications -Universal impedance bridge [2 Hrs]
arrangements to measure R, L,C

CRO

CRO- Block diagram and principle of operation of CRO- operation of CRT [2 Hrs]
Electrostatic focusing- Electrostatic deflection (no derivation)
Block diagram of vertical deflection system- Applications of CRO [2 Hrs]
Types of CRO- Block diagram and operation of dual trace CRO
Dual beam CRO - Comparison between dual trace and dual beam CRO [2 Hrs]
Digital storage Oscilloscope- Block diagram- advantages.
Block Diagram –working principle of Function Generator. [1 Hr]

UNIT V

TRANSDUCERS, SENSORS & TEST INSTRUMENTS **[15 Hrs]**

TRANSDUCERS

Transducers –Classification of transducers-active passive, analog/digital [2 Hrs]
Strain gauge –Types-uses.
Construction, operation and applications of photo electric transducer, [2 Hrs]
LVDT, RVDT and Load cell.
Principle of working of Thermocouple- Temperature measurement [2 Hrs]
using thermocouple - list of applications
Principle of working of Thermistor –Temperature measurement [2 Hrs]
using thermistors - Types (NTC, PTC) – List of applications.

SENSORS

IR range sensor – IR proximity sensor- Ultrasonic range sensor [2 Hrs]

Touch Sensor- industrial applications

TEST INSTRUMENTS

Digital voltmeter –Types (to list only) - Basic block diagram of DVM – [2 Hrs]

Block diagram of Digital multimeter-

Advantages over analog instruments - Block diagram of Digital frequency [3 Hrs]

Counter– Simple PC based Data Acquisition system – Block diagram

Revision and Test **[12 Hrs]**

TEXT BOOK:

S.No	Title	Author	Publisher with Edition
1.	Electrical Technology	B.L.Theraja	Division of Nirja constructions and development co. (P) Ltd., - 1994.
2.	Electric Circuit Theory	Dr. M. Arumugam, N. Premkumaran	KannaPublisher,Delhi -1997

REFERENCE BOOK:

S.No	Title	Author	Publisher with Edition
1.	Modern Electronic Instrumentation and Measurement Techniques	Albert D.Helfrick and Willam David cooper	Prentice Hall of India Pvt. Ltd., 1996
2.	Electrical and Electronic-Measurements and Instrumentation	A.K.Sawheney	Dhanpatrai and Sons -1993.
3.	Electronic- Measurements and Instrumentation	R.K.Rajput	S.Chand (Third Edition)-2009
4.	Electronic- Measurements and Instrumentation	Sanjay Talbar&AkhileshUpadhyaya	DhanpatRai Publications (p) Ltd-2004
5.	Electronic Instrumentation	Kalsi	Kalsi H S.Tata McGraw hill Education, 2004
6.	Measurement systems- Application and Design	Ernest O. Doebelin	McGraw hill -2004
7.	Transducers and Instrumentation	D.V.S.Murty	McGraw hill -2004
8.	Electrical & Electronics Measurements and instrumentation	UmeshSinha	Satyaprakashan Tech,1992

LEARNING WEBSITES

1. **https://www.allaboutcircuits.com/textbook/**
2. https://blog.feedspot.com/electronics_blogs/
3. https://www.electrical4u.com/
4. https://www.khanacademy.org/science/electrical-
5. **https://www.testandmeasurementtips.com/where-to-get-free-training-in-electronics- and-instrumentation/**

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C320.1	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C320.2	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C320.3	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C320.4	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C320.5	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C320	**15**	**15**	**10**	**10**	**10**	**10**	**15**	**15**	**10**	**10**
Correlation Level	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 330 PROGRAMMING IN 'C'

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester: 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	End Semester Examination	Total	
Programming in 'C'	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION OF HOURS:

UNIT	TOPIC	No. of HOURS
I	Program development and introduction to c	13
II	C Operator ,I/O Statement and Decision making	12
III	Arrays & strings & Functions	13
IV	Structures and unions, Dynamic Memory Management	12
V	"C" Programming	13
	Revision and Test	12
	TOTAL	**75**

COURSE DESCRIPTION

C' is the most widely used computer language, which is being taught as a core course. C is general-purpose structural language that is powerful, efficient and compact, which combines features of high-level language and low-level language. It is closer to both Man and Machine. Due to this inherent flexibility and tolerance it is suitable for different development environments. Due to these powerful features, C has not lost its importance and popularity in recently developed and advanced software industry. C can also be used for system level programming and it is still considered as first priority programming language. This course covers the basic concepts of C. This course will act as "programming concept developer" for students. It will also act as "Backbone" for subjects like OOPS, Visual Basic, Windows Programming, JAVA etc.

OBJECTIVES:

At the end of the Course, the students will be able to

- Define Program, Algorithm and flow chart
- List down and Explain various program development steps
- Write down algorithm and flow chart for simple problems.
- Describe the concepts of Constants, Variables, Data types and operators.
- Develop programs using input and output operations.
- Understand the structure and usage of different looping and branching statements.
- Define arrays and string handling functions.
- Explain user-defined functions, structures and union.
- To understand the dynamic data structure and memory management.
- Develop the simple C programs for finding the parameters of some electronic circuits and write C programs using graphic functions.

COURSE OUTCOMES

ECC 330 PROGRAMMING IN 'C'	
After successful completion of this course, the students should be able to	
C330.1	Explain the fundamentals of C programming and illustrate the flowchart and design an algorithm for a given problem and to develop C programs
C330.2	Apply C operators , I/O statements in developing conditional and iterative statements to write C programs
C330.3	Analyze different operations on arrays and strings, built- in function and user defined functions to develop the program.
C330.4	Utilize structures, unions and dynamic memory management in writing C programs.
C330.5	Develop the simple C programs for finding the parameters of some electronic circuits and C programs using graphics functions.

ECC 330 PROGRAMMING IN 'C'

UNIT I

PROGRAM DEVELOPMENT & INTRODUCTION TO C **[13Hrs]**

Program, Algorithm & flow chart:-Program development cycle [1 Hr]

Programming language levels & features.

Algorithm – Properties & classification of Algorithm, flow chart [1 Hr]

symbols, importance & advantage of flow chart [1 Hr]

Introduction to C: -

History of C – features of C [1 Hr]

Structure of C program – Compile, link & run a program. [1 Hr]

Diagrammatic representation of program execution process. [2 Hrs]

Variables, Constants & Data types:

C character set-Tokens- Constants- Key words – identifiers and Variables [1 Hr]

Data types and storage – Data type Qualifiers [1 Hr]

Declaration of Variables – Assigning values to variables- [1 Hr]

Declaring variables as constants-Declaring variables as volatile- [1 Hr]

Overflow & under flow of data. [1 Hr]

Flow Chart – simple interest – Positive or Negative Number - Odd Number [1 Hr]

or Even number

UNIT II

C OPERATORS, I/O STATEMENT and DECISION MAKING **[12 Hrs]**

C operators:-Arithmetic, Logical, Assignment .Relational, Increment [2Hrs]

and Decrement, Conditional, Bitwise, Special Operator precedence and Associativity.

C expressions – Arithmetic expressions – Evaluation of expressions- Type cast operator [2 Hrs]

I/O statements: Formatted input, formatted output, Unformatted I/O statements [2Hrs]

Branching:- Introduction – Simple if statement – if –else – else-if ladder [2 Hrs]

nested if-else-Switch statement – go statement. [2 Hrs]

Looping statements:- While, do-while statements, for loop, break &continue [2 Hrs]

statement.

UNIT III

ARRAYS AND STRINGS FUNCTIONS **[13 Hrs]**

Arrays:-Declaration and initialization of One dimensional, [1 Hr]
Two dimensional and Character arrays – Accessing array elements – [2 Hrs]
Programs using arrays.

Strings :-Declaration and initialization of string variables, Reading String, [2Hrs]
Writing Strings – String handling functions (strlen(),strcat(),strcmp()) –
String manipulation programs. [1Hr]

Built–in functions: -Math functions – Console I/O functions – [1 Hr]
Standard I/O functions – Character Oriented functions. [2 Hrs]

User defined functions:-Defining functions & Needs-, [1 Hr]
Scope and Life time of Variables, Function call, return values, [1Hr]
Storage classes, Category of function – Recursion. [2Hrs]

UNIT IV

STRUCTURES AND UNIONS, DYNAMIC MEMORY MANAGEMENT **[12 Hrs]**

Structures and Unions:-Structure – Definition, initialization, [2 Hrs]
arrays of structures, Arrays with in structures, structures within structures, [2 Hrs]
Structures and functions – Unions – Structure of Union – [2 Hrs]
Difference between Union and structure. [1 Hr]

Dynamic Memory Management:- Introduction – dynamic memory [2 Hrs]
Allocation – allocating a block memory (MALLOC) –
Allocating multiple blocks of memory (CALLOC) [2 Hrs]
Releasing the used space: free – altering the size of a block (REALLOC). [1 Hr]

UNIT V

"C" PROGRAMMING **[13 Hrs]**

Program to find Sum of Series using "while" loop- [2 Hrs]
Program to find Factorial of N numbers using functions- [2 Hrs]
Program to swap the values of two variables. [1 Hr]
Program to implement Ohms Law- [1 Hr]
Program to find Resonant Frequency of RLC Circuit [2 Hrs]
Program to find equivalent resistance of three resistances [2 Hrs]
Connected in series and parallel-
Program to draw the symbol of NPN transistor using Graphics- [2 Hrs]
Program to draw the symbol of diode using Graphics [1 Hr]

Revision and Test **[12 Hrs]**

TEXT BOOK:

S.No	Title	Author	Publisher with Edition
1.	Programming in ANSI C	E.Balaguruswamy	Tata Mc -Graw Hill New Delhi, Third Edition, 2010
2.	Introduction to computer graphics	N. Krishnamoorthy	Tata Mc -Graw Hill New Delhi, Second Edition, 2009

REFERENCE BOOK:

S.No	Title	Author	Publisher with Edition
1.	Programming and Problem solving using C	ISRD Group, Lucknow	Tata Mc- GrawHill, New Delhi Sixth Reprint , 2010
2.	Let us C	Yeswanth	Kanetkar BPB Publications , Fourth Revised Edition, 2007
3.	A TextBook on C	E.Karthikeyan	PHI Private Limited, New Delhi , 2008
4.	Programming in C	D.Ravichandran	New Age International Publishers, C, FirstEdition1996 Reprint2011
5.	Computer Concepts And Programming in C	Dr.S.S.Khandare	S.Chand& Company Ltd. New Delhi , First Edition 2010
6.	Complete Knowledge in C	SukhenduDey, DebobrataDutta	Narosa Publishing House, New Delhi, Reprint2010
7.	Programming in C	ReemaTheraja	Oxford University Press, First Edition 2011
8.	Practical C Programming	SteveOualline	O'Reilly, ShroffPublishers, Eleventh Indian Reprint Oct2010

LEARNING WEBSITES

1 http://www.coep.org.in/page_assets/594/fy.pdf

2. http://www.cse.iitm.ac.in/course_details.php?arg=Mjg=

3. https://www.u-aizu.ac.jp/sgu/info/files/docs/P02-Englishcourse.pdf

4. ht http://www.pvpsiddhartha.ac.in/autonomus14/1-

5. https://www.scribd.com/document/161565322/

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C330.1	**3**	**3**	**2**	**2**	**1**	**2**	**3**	**3**	**2**	**2**
C330.2	**3**	**3**	**2**	**2**	**1**	**2**	**3**	**3**	**2**	**2**
C330.3	**3**	**3**	**2**	**2**	**1**	**2**	**3**	**3**	**2**	**2**
C330.4	**3**	**3**	**2**	**2**	**1**	**2**	**3**	**3**	**2**	**2**
C330.5	**3**	**3**	**2**	**2**	**1**	**2**	**3**	**3**	**2**	**2**
C330	**15**	**15**	**10**	**10**	**5**	**10**	**15**	**15**	**10**	**10**
Correlation Level	**3**	**3**	**2**	**2**	**1**	**2**	**3**	**3**	**2**	**2**

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in our institution in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 340 ELECTRONIC DEVICES &CIRCUITS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 Weeks

Course	Instruction		Examination			
	Hrs/ Week	Hrs/ Semester	Marks			
Electric Devices and Circuits Practical	4	60	Internal Assessment	End Semester Examination	Total	Duration
			25	75	100	3Hrs

ALLOCATION OF MARKS

CIRCUIT DIAGRAM	:	20
CONNECTION	:	25
EXECUTION & HANDLING OF EQUIPMENT	:	15
OUTPUT / RESULT	:	10
VIVA – VOCE	:	05
TOTAL	**:**	**75**

COURSE DESCRIPTION

This course is designed to provide students with fundamental concepts of Electron Devices for hands on experience and analyze the physical construction, working and V-I characteristics of diodes, BJT ,FET, SCR, LED\, TRIAC, DIAC and photo transistor using breadboards . This practical fulfills the need for students to build the basic knowledge of various types of Components, Transistors, Amplifiers and oscillators.

OBJECTIVES :

- To identify the Identify and check the working condition of passive & active Components and devices.
- To construct and understand the V-I characteristics of Semiconductor diodes.
- To construct and understand the characteristics of different types of rectifiers.
- To construct and plot the characteristics of Transistors.
- To Construct and draw the frequency response of RC coupled amplifier.
- To construct and understand the V-I characteristics of switching devices.
- To Construct and draw the characteristics of LDR and phototransistor.
- To check the continuity of electronic components using multimeter and construct the simple circuits.

COURSE OUTCOMES

ECC 340 ELECTRONIC DEVICES &CIRCUITS PRACTICAL	
After successful completion of this course, the students should be able to	
C340.1	Identify and check the working condition of passive & active components and switches and construct semiconductor diodes, transistors ,amplifiers and analyze their characteristics.
C340.2	Construct different types of rectifiers and analyze their characteristics
C340.3	Construct and analyze the V-I characteristics of switching devices. (SCR,TRIAC,DIAC).
C340.4	Construct and analyze the characteristics of LDR and phototransistor.
C340.5	Make Use of multimeter to check the continuity and construct simple circuits using LEDS.

EQUIPMENTS REQUIRED

S.No	Name of the Equipment	Range	Required Nos.
1.	DC Regulated power supply	0-30V, 1A	10
2.	High Voltage Power Supply	0-250V, 1A	2
3.	Signal Generator	1MHz	4
4.	Dual trace CRO	20 MHz / 30MHz	5
5.	Digital Multi meter	-	10
6.	DC Voltmeter (Analog/Digital)	Different Ranges	15
7.	DC Ammeter (Analog/Digital)	Different Ranges	15

ECC 340 ELECTRONIC DEVICES &CIRCUITS PRACTICAL

Note: At least 5 experiments should be constructed using breadboard/soldering
STUDY EXPERIMENT (Not for Examination)
Identify and check the working condition of passive & active components and switches.

S.No	Name of the experiment	Course Outcome
1.	Construct and plot the VI characteristics of PN junction diode and find the cut-in voltage.	**C340.1**
2.	Construct and plot the VI characteristics of Zener diode and find the break down voltage.	**C340.1**
3.	Construct and plot the regulation characteristics (by varying either load or line voltage) of Half wave rectifier with and without filters.	**C340.2**
4.	Construct and plot the regulation characteristics (by varying either load or line voltage) of Full wave rectifier with and without filters.	**C340.2**
5.	Construct and plot the regulation characteristics (by varying either load or line voltage) of Bridge rectifier with filters.	**C340.2**
6.	Construct and draw the Input and output characteristics of CE Transistor configuration and find its input & output resistance.	**C340.1**
7.	Construct and draw the frequency response of RC coupled amplifier and determine the 3-db bandwidth.	**C340.1**
8.	Construct and plot the drain characteristics of JFET and find its pinch off voltage.	**C340.1**
9.	Construct and plot UJT characteristics and find its Ip and Vv.	**C340.1**
10.	Construct and draw SCR characteristics and find its break over voltage.	**C340.3**
11.	Construct and plot the DIAC characteristics.	**C340.3**
12.	Construct and plot the TRIAC characteristics.	**C340.3**
13.	Construct and draw the waveforms of positive clipper and clamper.	**C340.1**
14.	Construct and draw the characteristics of LDR.	**C340.4**
15.	Construct and draw the characteristics of a photo transistor	**C340.4**
16.	By using a multimeter check the given wire continuity, check 2 & 3way mains cord and identify line ground and earth point.	**C340.5**
17.	Construct a circuit to glow the different colour LED alternatively.	**C340.5**

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

a) Attendance : 5 marks – (Award of marks same as theory subjects)

b) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

c) Record writing : 10 marks

Total **25 marks**

LEARNING WEBSITES

1. https://www.quora.com/What-are-some-best-sites-to-learn-the-basic-of-electronics-for-Electronics-enginee

2. https://www.pannam.com/blog/free-resources-to-learn-electrical-engineering/

3. http://www.pvpsiddhartha.ac.in/autonomus1

4. http://www.circuitstoday.com/4-great-books-to-study-basic-electronics

5. http https://www.edx.org/course/circuits-and-electronics-1-basic-circuit-analysiss://www.scribd.com/document/161565322/

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C340.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C340.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C340.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C340.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C340.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C340	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**10**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

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ECC350 ELECTRICAL CIRCUITS AND INSTRUMENTATIONPRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 15 Weeks

Course	Instruction		Examination			
Electrical Circuits and Instrumentation Practical	Hrs. Week	Hrs Semester	Marks			
			Internal Assessment	End Semester Examination	Total	Duration
	4	60	25	75	100	3Hrs

ALLOCATION OF MARKS

CIRCUIT DIAGRAM	:	20
CONNECTION	:	25
EXECUTION & HANDLING OF EQUIPMENT	:	15
OUTPUT / RESULT	:	10
VIVA – VOCE	:	05
TOTAL	**:**	**75**

COURSE DESCRIPTION

This Practical enables the students with concepts and elements of DC, AC circuits and fundamentals of Electrical machines .The Practical also deals with concepts, principles and working of analog and digital electronic measuring instruments. The introduction of this Practical will enable the students to be well exposed to a wide area of various electronic measuring instruments and sensors through knowledge of the fundamentals of electrical circuits.

OBJECTIVES:

- To construct and understand Ohm's law and Kirchhoff's laws.
- To construct and understand the network theorems.
- To construct and learn about series and parallel resonance Circuits.
- To calibrate the ammeter and voltmeter.
- To test the performance of wheat stone bridge.
- To determine the amplitude and frequency values by using CRO.
- To determine the characteristics of thermocouple and thermistor.
- To test the performance of a photoelectric transducer.
- To test the performance of a load cell and LVDT.
- To measure the voltage rating using multimeter.
- Construct charger for cellphone.

COURSE OUTCOMES

ECC350 ELECTRICAL CIRCUITS AND INSTRUMENTATIONPRACTICAL	
After successful completion of this course, the students should be able to	
C350.1	Construct circuits using Ohm's law, Kirchoff's laws, network theorems and resonance and analyse the performance..
C350.2	Utilize electronic measuring devices and determine the unknown resistance value using wheat stone bridge and find the amplitude and frequency value using CRO.
C350.3	Construct and analyse the performance of various transducers. (Thermocouple, Thermistor, Load cell , LVDT and Photoelectric transducer)
C350.4	Interpret the calibration process of voltmeter and ammeter.
C350.5	Make Use of multimeter to measure the rating of transformer and construct Charger for cellphone.

EQUIPMENTS REQUIRED:

S. No	Name of the Equipments	Range	Required Nos
1.	DC regulated power supply	(0-30V),1A	8
2.	Signal generators	1MHZ	3
3.	Dual trace CRO	20MHZ	4
4.	DC Voltmeter	(0-15V)	8
5.	DC Ammeter	(0-300μA)	6
6.	DC Ammeter	(0-100mA)	8
7.	Digital Multimeter	-	4
8.	Galvanometer	-	1
9.	Decade Resistance Box	-	1
10	Thermocouple	-	1
11	Thermistor,	-	1
12	Load cell	-	1
13	LVDT	-	1
14	Photoelectric transducer	-	1

ECC350 ELECTRICAL CIRCUITS AND INSTRUMENTATIONPRACTICAL

LIST OF EXPERIMENTS

Note: Atleast 5 experiments should be constructed using breadboard/ soldering.

S.No	Name of the experiment	Course Outcome
1.	Construct a circuit to verify Ohm's law.	**C350.1**
2.	Construct a circuit to verify Kirchhoff's voltage and current law.	**C350.1**
3.	Construct a circuit to verify Super position theorem.	**C350.1**
4.	Construct a circuit to verify Thevenin's Theorem.	**C350.1**
5.	Construct a circuit to verify Norton's Theorem.	**C350.1**
6.	Construct a circuit to verify Maximum power transfer Theorem.	**C350.1**
7.	Construct and test the performance of series resonant circuit and parallel resonant circuit.	**C350.1**
8.	Calibrate the given ammeter and voltmeter.	**C350.4**
9.	Construct and test the performance of Wheatstone bridge.	**C350.2**
10.	Measure the amplitude and frequency of signals using dual trace CRO.	**C350.2**
11.	Measure the frequency and phase angle using CRO by Lissajous figure.	**C350.2**
12.	Test the performance of LVDT.	**C350.3**
13.	Measure strain using strain gauge.	**C350.3**
14.	Determine the characteristics of a thermistor	**C350.3**
15.	Test the performance of a load cell.	**C350.3**
16.	Study the rating of a Given Step down transformer and measure the input and output voltage using a digital multimeter.	
17.	Construct and test the 3V charger for cell phone	

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

a)Attendance	: 5 marks – (Award of marks same as theory subjects)
b)Procedure/ observation and tabulation/ Other Practical related work	: 10 marks
c)Record writing	: 10 marks
Total	**25 marks**

LEARNING WEBSITES

1. https://www.quora.com/What-are-some-best-sites-to-learn-the-basic-of-electronics-for-Electronics-enginee

2. https://www.pannam.com/blog/free-resources-to-learn-electrical-engineering/

3. https://www.testandmeasurementtips.com/where-to-get-free-training-in-electronics-and-instrumentation/

4. http://www.circuitstoday.com/4-great-books-to-study-basic-electronics

5. http https://www.edx.org/course/circuits-and-electronics-1-basic-circuit-analysiss://www.scribd.com/document/161565322/

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C350.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C350.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C350.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C350.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C350.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C350	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**10**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

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ECC360 PROGRAMMING IN 'C' PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester : 15 weeks

Course	Instruction		Examination			
	Hrs/Week	Hrs / Semester	Marks			Duration
			Internal Assessment	End semester Examination	Total	
Programming in 'C' Practical	5	75	25	75	100	3 Hrs

ALLOCATION OF MARKS

No.	Allocation	Marks
1	Writing Algorithm	20
2	Writing Program	20
3	Executing program	25
3	Result	05
4	Viva Voce	05
Total		75

COURSE DESCRIPTION:

This subject is a fundamental for the student to learn how to write a program in high level language. So it will be useful for Electronics and Communication Engineers to write coding and to develop the software. Further practice for writing simple program for Electronics application is insisted.

HARDWARE REQUIRMENT:

Desktop/laptop computers : 15 nos

Laser printer : 01 no

SOFTWARE REQUIREMENT:

C-compiler and editor

OBJECTIVES:

At the end of the Course, the students will be able to

- Analyze the given problem.
- Think the logic to solve the given problem.
- Describe the concepts of constants, variables, data types and operators.

- Develop programs using input and output operations.
- Write programs using different looping and branching statements.
- Write programs based on arrays.
- Write programs for solving simple equations used in circuit theory.

COURSE OUTCOMES

ECC360 PROGRAMMING IN 'C' PRACTICAL	
After successful completion of this course, the students should be able to	
C360.1	Interpret the basic structure of the C programming and analyze the given problems and develop programming in C language .
C360.2	Identify the logic to solve the given problem and explain the concepts of constants, variables, data types and operators.
C360.3	Develop programs using input and output operations.
C360.4	Develop programs using different looping ,branching statements and based on arrays.
C360.5	Develop programs for solving simple equations used in circuit theory and draw the symbols using graphics .

ECC 360 PROGRAMMING IN 'C' PRACTICAL

S.No	Name of the experiment	Course Outcome
1.	Write C language program to find the simple interest and compound interest.	C360.1
2.	Write C language program to print your college name 10 times.	C360.1
3.	Write C language program to find the solution of a quadratic equation.	C360.1
4.	Write C language program to find whether the given number is a positive number, negative number or zero.	C360.1
5.	Write C language program to find the sum of series using While loop.	C360.1
6.	Write C language program to perform the Arithmetic operation based on the numeric key press using switch case statement. (1-Addition, 2-Subtraction, 3 – multiplication, 4 - Division).	C360.2
7.	Write C language program to implement Ohms Law.	C360.3
8.	Write C language program to find factorial of given N numbers using function.	C360.4
9.	Write C language program to prepare the total marks for N students by reading the Name, Reg. No, Marks 1 to Marks 6 using array of structure.	C360.4
10.	Write C language program to swap the values of two variables.	C360.4
11.	Write C language program to calculate the equivalent resistance of three resistances connected in series and parallel.	C360.5
12.	Write C language program to calculate the equivalent Capacitance of three Capacitors connected in series and parallel.	C360.5
13.	Write C language program to find Resonant Frequency of RLC Series and Parallel Circuits.	C360.5
14.	Write C language program to find the power factor of series RL circuits.	C360.5
15.	Write C language program to find the Q factor for series and parallel resonant circuits.	C360.5
16.	Write C language program to draw the symbol of NPN transistor using Graphics.	C360.5
17.	Write C language program to draw the symbol of Diode using Graphics.	C360.5

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

d) Attendance : 5 marks – (Award of marks same as theory subjects)

e) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

f) Record writing : 10 marks

Total **25 marks**

LEARNING WEBSITES

1 https://www.learn-c.org/

2. https://www.includehelp.com/articles/top-5-websites-for-learning-c-programming-language.aspx

3. https://www.toptal.com/c/the-ultimate-list-of-resources-to-learn-c-and-c-plus-plus

4. https://hackr.io/tutorials/learn-c

5. https://www.codechef.com/c-programming

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C360.1	3	3	3	3	3	3	3	2	3	3
C360.2	3	3	3	3	3	3	3	2	3	3
C360.3	3	3	3	3	3	3	3	2	3	3
C360.4	3	3	3	3	3	3	3	2	3	3
C360.5	3	3	3	3	3	3	3	2	3	3
C360	15	15	15	15	15	15	15	10	15	15
Correlation Level	3	3	3	3	3	3	3	2	3	3

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

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ECC 370COMPUTER APPLICATIONS PRACTICAL FOR ELECTRONICS

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester : 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Computer Applications Practical In Electronics	4	60	25	75	100	3 Hrs

ALLOCATION OF MARKS

CONTENT	Max. Marks	
	Section I	Section II
Procedure	15	15
Execution	15	15
Result with printout	5	5
viva	5	
Total	75	

COURSE DESCRIPTION:

The Computer Application Practical in Electronics facilitates the necessary knowledge and skills regarding creating, working and maintaining the documents, analyzing the data with charts manipulation of databases, presentation of documents with audio visual effects in a computer and provides the latest tools and technologies in helping the students to fetch better employment.

SOFTWARE REQUIREMENTS

SECTION I

Operating System : Windows XP or Windows Vista or Windows 7 / Linux

Office Package : Microsoft office 2000 or Office 2003 or Office 2007/Open Office

SECTION II

SPICE simulation tools : PSPICE or Multisim or Lab VIEW / OrCAD / TINA

HARDWARE REQUIREMENTS

Desktop/Laptop Computer System : 15 Nos

Laser Printer : 1 No

OBJECTIVES:

On completion of the following exercises, the students must be able to

- Understand the Windows operating systems, word processing
- Analyze the spreadsheet
- Create and manipulate the database Prepare PowerPoint presentation
- Understand Internet concepts and usage of e-mail
- Understand simulation of characteristics of various electronic components using electronics device automation tools.

COURSE OUTCOMES

ECC 370COMPUTER APPLICATIONS PRACTICAL FOR ELECTRONICS	
After successful completion of this course, the students should be able to	
C370.1	Explain the Windows operating systems and word processing.
C370.2	Analyze the spreadsheet and create the exercises in the spreadsheet.
C370.3	Create and manipulate the database and Prepare PowerPoint presentation.
C370.4	Interpret the Internet concepts and usage of e-mail.
C370.5	Develop the Simulation of various electronic devices and analyse characteristics

ECC370 COMPUTER APPLICATIONS PRACTICAL FOR ELECTRONICS

SECTION I (C370.1)

Exercise in WINDOWS:

1. a. Install screen saver and change the monitor resolution by 1280X960
   b. Setting wall papers
   c. Creating, moving, deleting and renaming a folder
   d. Copying files into CD/DVD
   e. Recording and saving an audio file
   f. Set/Change the date and time.

Exercise in WORD PROCESSING:

2. Create a standard covering letter and use mail merge to generate the customized letters for applying to a job in various organizations. Also, create a database and generate labels for the applying organizations.

3. Create a news letter of three pages with two columns text. The first page contains some formatting bullets and numbers. Set the document background colour and add 'confidential' as the watermark. Give the document a title which should be displayed in the header. The header/ footer of the first page should be different from other two pages. Also, add author name and date/ time in the header. The footer should have the page number.

4. a.Restoring files and folders from recycle bin
   b.Creating Short cuts for folder/file
   c. Finding a file or folder by name
   d.Selecting and moving two or more files/folders using mouse
   e. Sorting folders/files

5. Creating the following table and perform the operations given below

ABC.PVT.LTD

Chennai

Production Summary of Various Units in every Quarter

Unit	Product –ID	Jan-Mar	Apr-junejuly- sept	Oct-Dec.	
Unit-I	57	234	50	74	125
Unit-II	142	236	126	175	251
Unit-III	213	541	216	60	43
Unit-IV	125	243	127	250	136
Unit-V	143	152	138	80	45

- Arrange Unit name as left align and other columns as right align
- Use doubled Border to the Summary Title and fill with 15% gray colour
- Implement merging and splitting two or more cells
- Give alternative forecolour for columns
- Print the above table

Exercises in SPREADSHEET (C370.2)

6. Create a table of records with columns as Name and Donation Amount. Donation amount should be formatted with two decimal places. There should be at least twenty records in the table. Create a conditional format to highlight the highest donation with blue colour and lowest donation with red colour. The table should have a heading.

7. Prepare line, bar and pie chart to illustrate the subject wise performance of the class for any one semester.

Exercise in DATABASE (C370.3)

8. Prepare a payroll for employee database of an organization with the following details: Employee Id, Employee name, Date of Birth, Department and Designation, Date of appointment, Basic pay, Dearness Allowance, House Rent Allowance and other deductions if any.
   Perform simple queries for different categories.

Exercise in POWER POINT (C370.3)

9. Create a Presentation on a mini project with ten different slide transitions with sound effect.

Exercise in INTERNET (C370.4)

10. a) Create e-mail id and perform the following.
    i. Write an e-mail inviting your friends to your birthday party.
    ii. Make your own signature and add it to the e- mail message.
    iii. Add a word attachment of the venue route
    b) Send the e-mail to at least 2 of your friends.

SECTION II (C370.5)

Exercises in SIMULATION TOOLS

11. Simulate VI characteristics of PN junction diode.
12. Simulate VI characteristics of LED.
13. Simulate VI characteristics of Zenerdiode.
14. Simulate VI characteristics of NPN transistor.
15. Simulate VI characteristics of FET.
16. Simulate VI characteristics of UJT.
17. Simulate VI characteristics of SCR.

LEARNING WEBSITES

1.https://www.makeuseof.com/tag/get-started-diy-electronic-projects-learning-sites

2. https://www.codecademy.com/

3. https://www.toptal.com/c/the-ultimate-list-of-resources-to-learn-c-and-c-plus-plus

4. https://hackr.io/tutorials/learn-c

5. https://www.codechef.com/c-programming

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C370.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**3**	**3**
C370.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**3**	**3**
C370.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**3**	**3**
C370.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**3**	**3**
C370.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**3**	**3**
C370 Total	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**5**	**15**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**1**	**3**	**3**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

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ECC 310 ELECTRONIC DEVICES &CIRCUITS
MODEL QUESTION PAPER

Time: 3Hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's Level**
1.	What is Semiconductor?	I	U
2.	Draw the symbol of Zener diode.	I	R
3.	What is biasing?	II	U
4.	What are Current gain and voltage gain of CB configuration?	II	R
5.	What is Barkhausen criterion?	III	U
6.	Draw the symbol for UJT.	III	R
7.	State Application of TRIAC.	IV	U
8.	What are the advantages of LCD?	V	U
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's Level**
9.	Explain the Operation of PN Junction Diode.	I	U
10.	Explain the Operation of Bridge Rectifier.	I	U
11.	How a transistor works as a switch? Explain.	II	U
12.	Compare FET and BJT.	III	R
13.	What are the characteristics of enhancement mode MOSFET?	IV	U
14.	Explain the Operation of SCR as switch.	IV	AP
15.	Explain the working of Phototransistor.	V	U
16.	Explain the working of solar cell.	V	U

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's Level**	**Max marks**
17.	**A.**	With suitable sketches, explain the operation of full wave rectifier.	I	U	10
		(OR)			
	B.	Explain the operation of Zener diode.	I	U	10
18	**A.**	Explain the input and output characteristics of common emitter configuration.	II	U	10
		(OR)			
	B.	Explain the principle of emitter follower and its application	II	U	10
19.	**A.**	Explain the Operation of Hartley Oscillator.	III	U	10
		(OR)			
	B.	With suitable sketches, explain the operation of FET amplifier.	III	U	10
20.	**A.**	Explain the working principle of SCR with neat diagram. Draw its VI characteristics.	IV	U	10
		(OR)			
	B.	Explain the speed control of fan using DIAC and TRIAC.	IV	AP	10
21.	**A.**	Describe the principle of operation of an LCD.	V	U	10
		(OR)			
	B.	With suitable sketches, explain the operation of an AstableMultivibrator.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECC 320 ELECTRICAL CIRCUITS AND INSTRUMENTATION
MODEL QUESTION PAPER

Time : 3 hrs **Max marks: 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's Level**
1.	What is meant by Current & Voltage?	I	U
2.	Define Ohm's law.	I	R
3.	Define power factor.	II	U`
4.	Define Resonance.	II	R
5.	What is ideal transformer?	III	U
6.	What are basic forces of indicating instruments?	IV	R
7.	Define voltmeter sensitivity.	IV	U
8.	What is a transducer? Give examples of transducer.	V	U
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's Level**
9.	Explain Kirchhoff's Voltage law and Current law.	I	U
10.	Derive the Voltage and Current relationship in pure capacitive circuit.	I	U
11.	Explain the losses in transformer.	II	U
12.	What are the applications of Stepper motor?	III	U
13.	Compare Dual Trace CRO & Dual Beam CRO.	IV	An
14.	Explain the construction of Thermistor.	IV	U
15.	Explain the applications of CRO.	V	U
16.	Explain load cell.	V	U

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's Level**	**Max marks**
17.	**A.**	State and explain Superposition Theorem.	I	U	10
		(OR)			
	B.	State and explain Maximum power transfer theorem.	I	U	10
18	**A.**	Derive an expression for the impedance in RLC series circuit.	II	An	10
		(OR)			
	B.	Derive the Q-factor of series resonant circuit.	II	An	10
19.	**A.**	Derive the E.M.F equation of a transformer.	III	An	10
		(OR)			
	B.	Explain the principle of operation of a D.C motor.	III	U	10
20.	**A.**	Explain the operation of Wheatstone bridge and state its applications.	IV	U	10
		(OR)			
	B.	Draw the block diagram of CRO and explain.	IV	U	10
21.	**A.**	Explain the block diagram of DVM.	V	U	10
		(OR)			
	B.	Explain the construction, operations & application of LVDT.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECC 330 PROGRAMMING IN 'C'
MODEL QUESTION PAPER

Time : 3 hrs **Max marks: 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's Level**
1.	What is flow chart?	I	U
2.	What is Variable?	I	R
3.	Define array.	III	U
4.	Define String.	III	R
5.	What are the types of function?	III	U
6.	Define Structure.	IV	R
7.	What is memory allocation?	IV	U
8.	What is Arithmetic operators ?	II	U
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's Level**
9.	Explain the flow chart symbols.	I	U
10.	Explain data type.	I	U
11.	Explain for Loop.	II	U
12.	Give any two needs of user defined functions.	III	R
13.	Give the different between array and structure.	IV	U
14.	Define a) Math function b) Console I/O function.	IV	U
15.	What is meant by Life time of variable?	V	U
16.	What do you mean by static memory allocation?	V	U

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's Level**	**Max marks**
17.	**A.**	Give the advantage of flowchart and draw flowchart to find the simple and compound interest.	I	U	10
		(OR)			
	B.	Explain the basic data type in 'C' and its modifiers.	I	U	10
18	**A.**	Explain operators	II	U	10
		(OR)			
	B.	Explain nested if statement with example.	II	U	10
19.	**A.**	Explain 1-D and 2-D array processing with example.	III	U	10
		(OR)			
	B.	Explain string handling function.	III	U	10
20.	**A.**	Explain array of structure with example.	IV	U	10
		(OR)			
	B.	Explain union with example.	IV	U	10
21.	**A.**	Write 'C' language programme to swap the values of two variables.	V	C	10
		(OR)			
	B.	Write a 'C' language programme to calculate to equivalent capacitance of three capacitors connected in series and parallel.	V	C	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECC 410 INDUSTRIAL ELECTRONICS

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
			Marks			
Industrial Electronics	Hrs/ Week	Hrs/ Semester	Internal Assessment	Semester End Examination	Total	Duration
	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME(HRS)
I	Power devices and Trigger circuits	13
II	Converters and choppers	13
III	Inverters and applications	13
IV	Programmable logic controller	12
V	DCS	12
Revision – Test		12
TOTAL		**75**

COURSE DESCRIPTION:

A program that prepares individuals to apply technical knowledge and skills to assemble, install, operate, maintain, and repair electrical/electronic equipment used in industry and manufacturing. Includes instruction in installing, maintaining and testing various types of equipment. The idea behind the modifying this subject is to give clear explanation of power devices and circuits that are widely used today in modern industry. It also gives exposure to PLCs & DCS which can perform various control functions in industrial environments.

OBJECTIVES:

On completion of the following units of the syllabus contents, the students must be able to

- Study working principle of MOSFET, IGBT
- Study the methods of triggering
- learn about converters and its types.
- understand commutation concepts in SCR
- learn about choppers.

- Study about inverters and types.
- understand the concept of HVDC.
- know about SMPS.
- understand about UPS and its types.
- learn about PLC.
- discuss about ladder diagrams.
- know about the architecture of DCS
- know about LCU and display units of DCS

COURSE OUTCOMES

ECC 410 INDUSTRIAL ELECTRONICS

After successful completion of this course, the students should be able to

C410.1 Explain the principle of working, VI characteristics and applications of power electronic devices - IGBT, MOSFET and GTO and learn triggering circuits.

C410.2 Explain the operation of converters and choppers.

C410.3 Infer the operation of inverter and describe its applications in SMPS and UPS.

C410.4 Analyze the basic concepts, logic function, input and output module, Ladder programming and applications of Programmable Logic Controller.

C410.5 Illustrate about distributed control systems.

ECC 410 INDUSTRIAL ELECTRONICS

UNIT- I

POWER DEVICES AND TRIGGER CIRCUITS **[13 Hrs]**

POWER DEVICES

Insulated gate bipolar transistor (IGBT), MOSFET and GTO [3Hrs]
Symbol, principle of working, VI characteristics and applications.
Comparison - between power MOSFET, power transistor and power IGBT [2Hrs]

TRIGGER CIRCUITS

Triggering of SCR - Gate triggering –Types –Concepts of DC triggering, [2 Hrs]

AC triggering, Pulse gate triggering – Pulse transformer in trigger circuit [3Hrs]

Electrical isolation by opto isolator

Resistance ,capacitor firing circuit and waveform, Synchronized [2Hrs]

UJT triggering (ramp triggering) circuit and waveform. [1 Hr]

UNIT -II

CONVERTERS AND CHOPPERS (Qualitative treatment only) **[13 Hrs]**

CONVERTERS

Converters – Definition – Single phase Half controlled bridge converter [2 Hrs]

with R load and RL load

Importance of flywheel diode –Single phase fully controlled bridge converter [3 Hrs]

with Resistive load – voltage and current waveforms

Single phase fully controlled bridge converter with RL load – [3 Hrs]

Voltage and current waveforms.

Commutation- Natural commutation – Forced commutation – Types [2 Hrs]

CHOPPERS

Chopper – Definition –principle of DC chopper operation – Typical chopper [2 Hrs]

Circuit (Jones chopper) –Applications of DC chopper

Principle of working of single phase AC chopper - Chopper using MOSFET. [1 Hr]

UNIT - III

INVERTERS & APPLICATIONS **[13 Hrs]**

INVERTERS

Inverter with resistive load [2 Hrs]

Single phase inverter with RL load –Methods to obtain sine wave output from [3 Hrs]

an inverter-output voltage control in inverters

McMurray inverter-Advantages-Parallel [2 Hrs]

INVERTERS APPLICATIONS

SMPS Types - Block diagram of SMPS – advantages and disadvantages. [3 Hrs]

UPS-Type (ON Line, OFF Line), Comparison - Battery banks [2 Hrs]

Parallel Inverter using IGBT and MOSFET [1 Hr]

UNIT -IV
PROGRAMMABLE LOGIC CONTROLLER **[12 Hrs]**

Evolution – Advantages over relay logic [2 Hrs]

Introduction to PLC – Relays- Block diagram of PLC

PLC Programming Languages - Arithmetic Functions – [2 Hrs]

(add, sub, mul, div, sqr) - Comparison of functions

Basics of Input and output module (digital input and output module) [2 Hrs]

Logic functions - AND logic, OR logic, NAND logic, EX-OR logic [2 Hrs]

Symbols used in ladder logic diagram.

Ladder programming – Ladder diagram for simple Systems [2 Hrs]

Star delta starter, Conveyer control and Lift control [1 Hr]

PLC interface with GSM [1 Hr]

UNIT -V
DISTRIBUTED CONTROL SYSTEMS **[12 Hrs]**

Evolution - Hybrid system Architecture [2 Hrs]

Central system Architecture [2 Hrs]

Generalized Distributed Control – Architecture [2 Hrs]

Comparison of architectures [2 Hrs]

Local control unit – Basic Elements of LCU [1 Hr]

Displays – Plant – Area – Group - Loop [2 Hrs]

Features of DCS – Advantages of DCS [1 Hr]

Revision and Test **[12 Hrs]**

TEXT BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Power Electronics	M.H.Rashid	PHI Publication-3rd Edition-2005
2.	Industrial Electronics and control	Biswanath Paul	PHI publications-2nd Edition -2010
3.	Programmable Logic Controllers	Frank D.Petruzela	PHI publications -4th Edition -2010
4.	Power Electronics	Dr.P.S.Bimbhra	Khanna publishers -2nd Edition-1998

REFERENCE BOOKS:

S.NO	TITLE	AUTHOR	PUBLISHER WITH EDITION
1.	Industrial & Power Electronics	Harish C.Rai	Umesh Publication, 5th Edition 1994
2.	'Programmable Logic Controllers – Principles and applications	John W. Webb. Ronald A. Reis	PHI publications 2017
3.	Programmable Logic Controller	Pradeep Kumar& Srivashtava	BPB Publications 2004

LEARNING WEBSITES

1. **https://www.quora.com/What-are-the-best-websites-for-power-electronics-and-power-systems**
2. **https://www.udemy.com/fundamentals-of-power-electronics-1/**
3. https://www.powerelectronictips.com/dozen-best-web-sites-for-power-electronics-
4. **https://interestingengineering.com/10-best-websites-for-electrical-engineering-students**
5. **https://www.electronics-tutorials.ws/**

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C410.1	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**1**	**1**
C410.2	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**1**	**1**
C410.3	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**1**	**1**
C410.4	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**1**	**1**
C410.5	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**1**	**1**
C410	**15**	**10**	**10**	**10**	**10**	**10**	**15**	**15**	**5**	**5**
Correlation Level	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**3**	**1**	**1**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs) R-Remember, U-Understand , Ap-Apply	Higher Order Thinking Skills (HOTs) An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 420 COMMUNICATION ENGINEERING

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
	Hrs/ Week	Hrs/ semester	Marks			Duration
			Internal Assessment	semester End Examination	Total	
Communication Engineering	5	75	25	75	100	3Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME(HRS)
I	Networks, Antenna and Propagation	13
II	Introduction to Modulation and Amplitude Modulation	13
III	Frequency and Pulse Modulation	13
IV	Audio Systems	12
V	Video Systems	12
	Revision Test	12
	TOTAL	**75**

COURSE DESCRIPTION:

Today communication engineering has developed to a great extent that there is always the need for study of various communication concepts. This subject fulfills the need for students to have a thorough knowledge of various types of networks, modulation, audio systems and video systems.

OBJECTIVES

On completion of the following units of syllabus contents, the students must be able to:

- Understand the principle of working of antenna
- Understand the theory of Propagation
- Understand the concept of modulation
- Study amplitude modulation process
- Learn about different types of AM Transmitter and Receiver:
- Study the Frequency modulation process
- Learn about different types of FM Transmitter and Receiver:
- Understand the concept of Phase modulation
- Understand the concept of Pulse modulation
- Learn different types of loud speakers
- Understand different methods of Audio Recording and Reproduction
- Learn different types of Microphones
- Understand principles of Monochrome color TV and Related topics

COURSE OUTCOMES

ECC 420 COMMUNICATION ENGINEERING

After successful completion of this course, the students should be able to

C420.1 Summarize the basic concepts of antennas, filters, equaliser, attenuator and different types of wave propagation.

C420.2 Organize the fundamentals of Modulation ,Amplitude Modulation , spectrum, signal diagram, AM transmitter and AM receiver.

C420.3 Explain the fundamentals of Frequency Modulation ,spectrum ,signal diagram and different types of pulse modulation.

C420.4 Illustrate the basic concepts of audio systems – Microphones, Loud speakers ,Audio recording and reproduction.

C420.5 Show the knowledge on video systems and learn about Monochrome , Colour television and Digital Television Systems.

ECC 420 COMMUNICATION ENGINEERING

UNIT-I

NETWORKS, ANTENNA AND PROPAGATION **[13 Hrs]**

NETWORKS :

Symmetrical and asymmetrical networks [2 Hrs]

characteristic impedance and propagation constant [2 Hrs]

Equaliser: Definition, types and applications [2 Hrs]

Attenuator: Definition - types - symmetrical T and Pi attenuators- application & Simple problems [2 Hrs]

Filters: Definition - types - circuit elements and cutoff frequencies of LPF, HPF and BPF (only simple problems) – applications [2 Hrs]

Antennas: Definition – types of antenna: Mono pole and dipole antenna, directional and omni directional antenna ,Dipole arrays, Yagi antenna- parabolic antenna. Antenna parameters: directive gain, directivity, radiation pattern and polarization- applications. [2 Hrs]

Propagation: Ground wave propagation- sky wave- space wave propagation [1 Hr]

UNIT - II
INTRODUCTION TO MODULATION AND

AMPLITUDE MODULATION **[13 Hrs]**

Introduction to Modulation: Definition - Need for modulation- [2 Hrs]

types of modulation-Frequency Spectrum – Relationship between Wavelength and frequency [2 Hrs]

Amplitude modulation: Definition - Simple signal diagram for amplitude modulation Expression for amplitude modulation [2 Hrs]

Expression for modulation index - sidebands: DSB, SSB and VSB. [2 Hrs]

AM Transmitter: Types of transmitters - high level AM transmitter and low level AM transmitter-SSB transmitter. [2 Hrs]

AM Receiver: Types of receiver: TRF receiver- super heterodyne radio receiver and SSB receiver-Selection of IF-AGC types- Simple and delayed AGC. [3 Hrs]

UNIT- III

FREQUENCY AND PULSE MODULATION **[13 Hrs]**

Frequency modulation: Definition - Simple signal diagram for frequency [2 Hrs]
Modulation –Expression for frequency modulation
Expression for modulation index
FM threshold and its extension, Pre-emphasis and De-emphasis in FM [1 Hr]

FM Transmitters : Types of transmitters : Direct FM transmitter, [2 Hrs]
Indirect FM transmitter and stereophonic FM transmitter. [2 Hrs]
FM Receiver: stereophonic FM receiver - AFC – [3 Hrs]
Comparison of FM and AM.
Pulse modulation: Definition – types - Generation and [3 Hrs]
detection of PAM- PWM- PPM,PCM and DPCM

UNIT -IV

AUDIO SYSTEMS **[12 Hrs]**

Microphones: Definition-Construction and performance of the following [3 Hrs]
microphones: carbon- condenser- piezo-electric- moving coil and velocity ribbon.
Loud speakers: Definition-Constructional details of dynamic cone type- [3 Hrs]
Horn type and electro-static loud speakers- [2 Hrs]
woofer midrange and tweeter cross-over network. Surround-sound systems
Audio recording and reproduction: Compact disc system- MP3 system [2 Hrs]
- DVD system
stereophonic system - Hi-Fi system principles- DTS [2 Hrs]

UNIT – V

VIDEO SYSTEMS **[12 Hrs]**

Monochrome Television: Scanning principles [3 Hrs]
synchronization - aspect ratio- composite video signal
TV broadcasting standards- TV transmitter - TV receiver [3 Hrs]
Colour TV : Principles of colour transmission and reception- [3 Hrs]
colour CCD camera
LCD, LED display unit – plasma display - Principles of Handy cam [2 Hrs]
CCTV and cable TV.
Digital Television Systems [1 Hr]
Revision and Test **[12 Hrs]**

TEXT BOOKS:

Sl.No	Title	Author	Publisher with Edition
1.	Transmission Lines & Networks	Umesh Sinha	Sathya Prakashan Publications – 5th edition 1992
2.	Radio Engineering - I	G.K.Mitha	Khana Publisher – 7th edition 1992

REFERENCE BOOKS:

Sl.No	Title	Author	Publisher with Edition
1.	Networks lines and fields	John D.Ryder	PHI ,II Edition 2005
2.	Electronic communication Systems	George Kennedy	TMH, 10 th reprint 2011
3.	Electronic Communication	Dennis Roddy John colen	PHI, II Edition 2005
4.	Fundamentals of Acoustics	Kingsler & frey	Wiley Eastern Ltd. 2 nd edition 1967
5.	TV and Video engineering	Arvind M.Dhake	TMH, 15 th reprint 2005.
6.	Communication Electronics – Principles and application -	Louis E Frenzel	Third Edition, Tata McGrawhill publication 2002
7.	Audio and Video system - – Principles, maintenance and Troubleshooting	R.Gupta	Second Edition McGrawHill Education (P) Ltd-2010

LEARNING WEBSITES

1.https://study.com/directory/category/Engineering/Electrical_Engineering_and_Electronics/Electronic_Comı unications_Engineering.html

2. https://www.udemy.com/topic/electronics/

3. http://www.engineersdream.com/10-free-websites-tools-learn-electronics-tutorials/

4. https://interestingengineering.com/10-best-websites-for-electrical-engineering-students

5 https://www.gadgetronicx.com/best-websites-to-learn-build-electronics/

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C420.1	**3**	**3**	**3**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C420.2	**3**	**3**	**3**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C420.3	**3**	**3**	**3**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C420.4	**3**	**3**	**3**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C420.5	**3**	**3**	**3**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C420	**15**	**15**	**15**	**10**	**10**	**10**	**15**	**15**	**10**	**10**
Correlation Level	**3**	**3**	**3**	**2**	**2**	**2**	**3**	**3**	**2**	**2**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs) R-Remember, U-Understand , Ap-Apply	Higher Order Thinking Skills (HOTs) An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 430 DIGITAL ELECTRONICS

TEACHING AND SCHEME OF EXAMINATION

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
	Hrs/ Week	Hrs / Semester	Marks			Duration
			Internal Assessment	semester End Examination	Total	
Digital Electronics	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION

UNIT	TOPIC	TIME (Hrs)
I	Number System, Boolean Algebra, Logic Gates and Digital Logic Families	13
II	Combinational Logic	13
III	Sequential Logic	13
IV	Memory Devices	12
V	Microprocessor – 8085	12
	Revision Test	12
	TOTAL	**75**

COURSE DESCRIPTION:

The subject of Digital Electronics holds applications in all branches of engineering. This subject will impart in depth knowledge of Number systems, Logics of Combinational & Sequential circuits and also about various & recent Memory devices and microprocessor. The concept of Digital Electronics will be implemented in all processor.

OBJECTIVES :

- To understand various Number System.
- To understand basic Boolean postulates and laws.
- To understand the De-Morgan's theorem.
- To understand the concept of Karnaugh Map.
- To Learn about Basic logic Gates.
- To Study about Boolean techniques.
- To learn the different digital logic families
- To learn arithmetic circuits-adder/subtractor , BCD adder.
- To understand the encoder/decoder & MUX / DEMUX
- To understand the concept of parity Generator, and checkers
- To understand various types of flip-
- To understand various types of counters.
- To understand various modes of shift registers
- To understand the concept of RAM & ROM and its types.
- To understand the history and need of Microprocessor.
- To understand the internal architecture details of 8085 Microprocessor.
- To know the instruction set of 8085
- To understand Interrupt Structure of 8085

COURSE OUTCOMES

ECC 430 DIGITAL ELECTRONICS	
After successful completion of this course, the students should be able to	
C430.1	Explain the conversion of different type of codes and number systems which are used in digital communication ,computer systems and understand different types of logic gates and logic families .
C430.2	Analyze different types of digital combinational circuits like adder, subtractor, Decoder, Encoder ,multiplexer, demultiplexer, Parity Checker and generator
C430.3	Develop competence in analysis of sequential circuits like flip –flops, counters and different types of Registers.
C430.4	Distinguish between the different types of memory devices like RAM, ROM,EPROM,EEPROM, FLASH memory and antifuse technology.
C430.5	Interpret the evolution of microprocessor, architecture of 8085 ,addressing modes, instruction sets and interrupts.

ECC 430 DIGITAL ELECTRONICS

UNIT - I

NUMBER SYSTEM AND BOOLEAN ALGEBRA **[13 Hrs]**

Binary, Octal, Decimal, Hexadecimal - Conversion from one to another. [2 Hrs]

Binary codes – BCD code, Gray code, Excess 3code.Boolean Algebra [1 Hr]

Boolean postulates and laws. De-Morgan's theorem [2 Hrs]

Simplification of Boolean expressions using Karnaugh map (up to 4 variables-pairs, quad, octets) - Don't care conditions and constructing the logic circuits for the Boolean expressions [2 Hrs]

LOGIC GATES AND DIGITAL LOGIC FAMILIES:

Gates – AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR [1 Hr]

Implementation of logic functions using gates, Realization of gates using universal gates. [2 Hrs]

Simplification of expression using Boolean techniques, [1 Hr]

Boolean expression for outputs

Digital logic families - Fan in, Fan out, Propagation delay ,TTL [2 Hrs]

CMOS Logics and their characteristics - comparison and applications

Tristate logic

UNIT -II

COMBINATIONAL CIRCUITS **[13 Hrs]**

Arithmetic circuits - Binary – Addition, subtraction, 1's and 2's complement. [2 Hrs]

Signed binary numbers.

Half Adder and Full Adder [2 Hrs]

Half Subtractor and Full Subtractor. [2 Hrs]

Parallel and serial Adders- BCD adder.

Encoder, Decoder [2 Hrs]

3to 8 decoder, BCD to seven segment decoder [2 Hrs]

Multiplexer - basic 2 to 1 MUX, 4 to 1 MUX, 8 to 1 MUX – applications of the MUX – Demultiplexer - 1 to 2 demultiplexer, [2 Hrs]

1 to 4 demultiplexer, 1 to8 demultiplexer - Parity Checker and generator. [1 Hr]

UNIT- III

SEQUENTIAL CIRCUITS	**[13 Hrs]**
FLIP -FLOPS – SR, JK, T, D FF	[2 Hrs]
JK- MS FF, Triggering of FF – edge & level	[2 Hrs]
Counters – 4 bit Up - Down Asynchronous / ripple counter, Decade counter	[1 Hr]
Mod3, Mod7 counter, 4 bit Synchronous Up – Down counter	[2 Hrs]
Johnson counter, Ring counter	[1 Hr]

REGISTERS

4-bit shift register- Serial IN Serial OUT	[2 Hrs]
Serial IN parallel OUT	[1 Hr]
Parallel IN Serial OUT	
Parallel IN Parallel OUT	[2 Hrs]

UNIT-IV

MEMORY DEVICES	**[12 Hrs]**
Classification of memories, RAM organization - Address Lines and Memory Size, Read/write operations	[3 Hrs]
Static RAM - Bipolar RAM cell, Dynamic RAM	[2 Hrs]
SD RAM, DDR RAM. Read only memory – ROM organization	[2 Hrs]
Expanding memory, PROM	[2 Hrs]
EPROM, and EEPROM	[2 Hrs]
Flash memory, Anti Fuse Technologies	[1 Hr]

UNIT -V

MICROPROCESSOR – 8085	**[12 Hrs]**
Evolution of microprocessor 8085 – Architecture of 8085	[2 Hrs]
Pin diagram of microprocessor 8085	[2 Hrs]
Instruction sets	
Addressing modes	[2 Hrs]
Memory mapped I/O and I/O mapped I/O and its Comparison	[1 Hr]
Machine cycle – Opcode fetch, memory read, memory write	[1 Hr]
I/O read, I/O write	[1 Hr]
Instruction cycle (Timing diagram) for MOV r1, r2 instructions	[2 Hrs]
Interrupts (types & Priorities)	[1 Hr]

Revision and Test	**[12 Hrs]**

TEXT BOOKS:

Sl.No	Title	Author	Publisher with Edition
1.	Principles of Digital Electronics	K.Meena	PHI – 2011
2.	Modern Digital Electronics	R.P.Jains	TMH -2003
3.	Microprocessor architecture programming and application	Ramesh S. Gaonkar	Wiley Eastern Limited. 2rd Edition 2002

REFERENCE BOOKS:

Sl.No	Title	Author	Publisher with Edition
1.	Digital principles & Applications	Albert Paul Malvino & Donald P.Leach	TMH - 4th Edition 2002
2.	Digital Electronics	William H.Gothmann	prentice Hall of India – 2nd Edition, 1995
3.	Introduction to Microprocessor	Aditya P Mathur	Tata McGraw-Hil publishing Company Limited 1989
4.	Digital Electronics	Roger L.Tokheim Macmillan	McGraw hill -1994
5.	Digital Electronics- an introduction to theory and practice	William H.Gothmann	PHI 1998

LEARNING WEBSITES

1. https://www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/
2. https://www.tutorialspoint.com/digital_electronics/index.asp
3 https://en.wikibooks.org/wiki/Digital_Electronics
4. https://www.electrical4u.com/digital-electronics/
5 .https://www.factmonster.com/dk/encyclopedia/science/digital-electronics

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C430.1	3	3	3	2	2	2	3	3	1	2
C430.2	3	3	3	2	2	2	3	3	1	2
C430.3	3	3	3	2	2	2	3	3	1	2
C430 .4	3	3	3	2	2	2	3	3	1	2
C430 .5	3	3	3	2	2	2	3	3	1	2
C430	15	15	15	10	10	10	15	15	5	10
Correlation Level	3	3	3	2	2	2	3	3	1	2

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs) R-Remember, U-Understand , Ap-Apply	Higher Order Thinking Skills (HOTs) An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC440 LINEAR INTEGRATED CIRCUITS

TEACHING AND SCHEME OF EXAMINATION

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	semester End Examination	Total	
Linear Integrated Circuits	4	60	25	75	100	3 Hrs

TOPICS AND ALLOCATION

UNIT	TOPIC	TIME (Hrs)
I	Introduction to operational amplifiers	10
II	Opamp applications	10
III	PLL & Waveform generators	9
IV	D/A and A/D Converters	10
V	Special Function ICS	9
	Revision Test	12
	TOTAL	**60**

COURSE DESCRIPTION:

This is a course on the design and applications of operational amplifiers and analog integrated circuits. This course introduces basic op-amp principles and show how the op-amp can be used to solve a variety of application problems. Much attention is given to basic op-amp configurations, linear and non-linear applications of op-amp and active filter synthesis, including switched capacitor nfigurations. It also deals with oscillators, waveform generators and data converters. IC technology needs the fundamentals of Integrated Circuits for students regarding the application and special function ICs.

OBJECTIVES

- To understand the basics of operational amplifier.
- To study the op-amp applications.
- To understand PLL & waveform generators.
- To study D/A and A/D converters and special function ICs.
- To design of special IC'S in Astable multivibrator ,Bistable multivibrator and general purpose regulators.

COURSE OUTCOMES

ECC 440 LINEAR INTEGRATED CIRCUITS	
After successful completion of this course, the students should be able to	
C440.1	Summarize the basic concepts of operational amplifier ,its various applications and manufacturing process.
C440.2	Infer about the OP-AMP applications and waveform generators.
C440.3	Explain the operation of PLL and its applications.
C440.4	Illustrate knowledge on D/A , A/D converters and their specifications.
C440.5	Explain the operation of IC 555, its applications and learn about IC voltage regulators.

ECC440 LINEAR INTEGRATED CIRCUITS

UNIT I

INTRODUCTION TO OPERATIONAL AMPLIFIERS **[10 Hrs]**

Integrated circuit – classification of IC - Advantages of IC over discrete [2 Hrs]

components –Types of IC Packages – Operational amplifier IC 741 [1 Hr]

Schematic symbol for opamp – pin diagram of IC 741

Block diagram of an opamp [1 Hr]

Characteristics of an Ideal opamp - Simple Equivalent circuit of an opamp [1 Hr]

virtual ground – opamp parameters – CMRR –Slewrate [2 Hrs]

Basic linear circuits- Inverting Amplifier, Non Inverting amplifier [2 Hrs]

Differential Amplifier – sign changer – scale changer.

Manufacturing process of monolithic ICs [1 Hr]

UNIT –II

OPAMP APPLICATIONS **[10 Hrs]**

Summing amplifier - Multiplier – Divider – Voltage follower – comparator [2 Hrs]

zero crossing detector - Integrator – Differentiator – Voltage to current converter [2 Hrs]

current to voltage converter –Instrumentation amplifier [2 Hrs]

Sign Changer, Scale Changer [1 Hr]

Waveform generators – square wave, triangular wave, sine wave [2 Hrs]

saw tooth wave generators (Qualitative treatment only) [1 Hr]

UNIT –III

PLL & APPLICATIONS (Qualitative treatment only) **[9 Hrs]**

PLL – Basic principles of PLL – Basic Block schematic of PLL – Lock range [2 Hrs]

capture range – Basic components of PLL – Phase detector – LPF – VCO [2 Hrs]

Monolithic VCO 566 - Pin diagram [1 Hr]

Basic Block diagram of VCO 566 - Monolithic PLL 565 - pin diagram [2 Hrs]

Functional Block diagram of PLL IC 565 - Applications of PLL [2 Hrs]

Frequency translation – frequency multiplication.

UNIT –IV

D/A AND A/D CONVERTERS **[10 Hrs]**

D/A CONVERTERS:

Digital to analog converter – Basics of D/A conversion – weighted Resistor	[1 Hr]
D/A Converter - R-2R Ladder D/A Converter –Specifications of DAC	[1 Hr]
Accuracy, Resolution, Monotonicity, Settling time.	[1 Hr]

A/D CONVERTERS:

Analog to digital converter – Basics of A/D conversion – sampling	[2 Hrs]
Sample and hold circuit – quantization – Types of A/D converter	[1 Hr]
Block diagram of Flash, Successive approximation, Ramp	[1 Hr]
Dual Slope ADC – Specifications of ADC – Accuracy, Resolution,	[2 Hrs]
Conversion time – Functional Block diagram of IC ADC 0808.	[1 Hr]

UNIT –V

SPECIAL FUNCTION ICs (Qualitative treatment only) **[9 Hrs]**

IC 555 Timer – pin diagram of IC 555 – Functional Block diagram of IC555	[2 Hrs]
Applications – Astable multivibrator – monostable multivibrator	[1 Hr]
Schmitt trigger - IC voltage regulators	[2 Hrs]
Linear fixed voltage regulator - Positive voltage regulator using IC 78xx	[1 Hr]
Negative voltage regulator using IC 79xx	[1 Hr]
General purpose regulator using LM 723 – Pin diagram of LM 723	[1 Hr]
Low voltage and High - voltage regulator using LM 723.	[1 Hr]

Revision and Test **[12 Hrs]**

TEXT BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Linear Integrated circuits	D.Roy choudhury & Shail.B. Jain .	New age International Publishers – II Edition – 2005
2.	Integrated circuits	K.R. Botkar	Khanna Pulbisher's – 1996

REFERENCE BOOKS:

Sl.No	Title	Author	Publisher with Edition
1	Introduction to system design using IC	B.S. Sonde	Wiley Eastern Limited II Edition -1992
2	Operational Amplifiers and Linear Integrated circuits	Ramakant .A Gayakwad	Prentice Hall – 2000
3	Digital Integrated Electronics	Taub & Schlling	Mcgraw Hill – 1997
4	Operational amplifiers and Linear Integrated circuits	Robert F.Coughlin and Frederick F.Driscol	PHI –publications –sixth Edition-2009
5	Linear Integrated Circuits	Salivahanan V.S.Kanchana Baskaran	TMH-2008

LEARNING WEBSITES

1. https://whatis.techtarget.com/definition/linear-integrated-circuit-linear-IC
2.https://www.tutorialspoint.com/linear_integrated_circuits_applications/basics_of_linear_integrated_circuits_applications.htm
3 https://www.tutorialspoint.com/linear_integrated_circuits_applications/index.htm
4 .http://www.eeeguide.com/introduction-to-linear-integrated-circuits/
5 . ttps://books.google.com/books/about/LINEAR_INTEGRATED_CIRCUITS.html?id=7Qt6l18wM7oC

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C440.1	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C440.2	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C440.3	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C440.4	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C440.5	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**
C440	**15**	**15**	**10**	**10**	**10**	**10**	**15**	**15**	**10**	**10**
Correlation Level	**3**	**3**	**2**	**2**	**2**	**2**	**3**	**3**	**2**	**2**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs) R-Remember, U-Understand , Ap-Apply	Higher Order Thinking Skills (HOTs) An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 450 INDUSTRIAL ELECTRONICS AND COMMUNICATION ENGINEERING PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester : 15 weeks

Course	Instruction		Examination			
	Hrs/ Week	Hrs/ semester	Marks			Duration
			Internal Assessment	Semester End Examination	Total	
Industrial Electronics and Communication Engineering Practical	5	75	25	75	100	3Hrs

ALLOCATION OF MARKS

CIRCUIT DIAGRAM	:20
CONNECTION	:20
EXECUTION & HANDLING OF EQUIPMENT	:20
OUTPUT / RESULT	:10
VIVA – VOCE	:05
TOTAL	**:75**

Course Description

Today communication engineering has developed to a great extent that there is always the need for study of various communication concepts. This lab fulfills the need for students to have a through knowledge of various types of networks, modulation, audio systems, industrial electronics concepts.

OBJECTIVES

At the end of the course , the students will be able to,

- Construct and test commutation circuits of SCR, TRIAC, MOSFET based PWM chopper circuit.
- Implementing logic program using digital inputs /output ,conveyor control and lift control.
- Construct & test symmetrical T & Pi attenuators and constant k passive low pass filter & high pass filter.
- Construct & test AM modulator and Detector circuit and FM modulator circuit and trace the output waveform
- Construct and test PAM generation circuit and detection circuit.
- Construct and test PWM,PCM generation circuit and detection circuit

COURSE OUTCOMES

ECC 450	**INDUSTRIAL ELECTRONICS AND COMMUNICATION ENGINEERING PRACTICAL**
After successful completion of this course, the students should be able to	
C 450.1	Demonstrate the ability to explore the characteristics of various power electronics devices by hands on.
C 450.2	Apply the PLC concepts in lift control ,conveyor control and simulate simple inputs and outputs, implement ladder logic diagram using timer and counter with PLC.
C 450.3	Construct and test the attenuators and filters which are used in communication circuits.
C 450.4	Construct and trace the waveforms of AM modulation /detection, PAM and PPM Generation/detection.
C 450.5	Build the frequency response of (low ,medium and high) of three way cross over network used in communication circuits.

EQUIPMENT REQUIRED:

S.No	Name of the Equipments	Range	Required Nos
1.	DC regulated power supply	(0-30V)	05
2.	Dual trace CRO	-	02
3.	Signal generators	-	02
4.	PAM Kit	-	01
5.	PCM Kit	-	01
6	PLC kits	-	02
7.	PPM Generation circuit & Detection	-	01
8.	Three way cross over network	-	01
9.	Computers	-	02

ECC 450 INDUSTRIAL ELECTRONICS AND COMMUNICATION ENGINEERING PRACTICAL

INDUSTRIAL ELECTRONICS LAB

S.No	Name of the experiment	Course Outcome
1.	Phase control characteristics of SCR and testing a commutation circuit.	C450.1
2.	Construct a Lamp dimmer using TRIAC (in Bread Board Only)	C450.1
3.	Construct and test a MOSFET based PWM chopper circuit	C450.1
4.	Construct and test an IC based buck converter using PWM	C450.1
5.	Write and implement a simple ladder logic program using digital inputs and outputs for PLC	C450.2
6.	Write and implement a simple ladder logic program for interfacing a lift control with PLC.	C450.2
7.	Write and implement a simple ladder logic program for interfacing a conveyer control with PLC	C450.2
8.	Write and implement a simple ladder logic program using timer and counter with branching and subroutines with PLC.	C450.2

COMMUNICATION ENGINEERING LAB

S.No	Name of the experiment	Course Outcome
9.	Construct & test Symmetrical T attenuators	C450.3
10.	Construct & test Symmetrical Pi attenuators	C450.3
11.	Construct & test Constant K Passive Low Pass Filter	C450.3
12.	Construct & test Constant K High Pass Filter	C450.3
13.	Construct an AM modulator and Detector circuit and trace the output waveform.	C450.4
14.	Construct & test PAM Generation circuit & Detection circuit	C450.4
15.	Construct & test PPM Generation circuit & Detection circuit.	C450.4
16.	Construct & Test a Three way cross over network	C450.5

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LEARNING WEBSITES

1. **https://ceme.ece.illinois.edu/files/2014/07/ECE469V25.pdf**
2. **https://www.researchgate.net/publication/263991124_Undergraduate_Power_Electronics_Laboratory_-_Applying_TSMST_Method**
3. **https://www.scribd.com/doc/212398780/Industrial-Electronics-Lab-Manual**
4. **http://ggnindia.dronacharya.info/EEE/Downloads/Labmanuals/IV_SEM_LAB_MANUAL/Principles_of_Communication_Systems_Lab_EE-230-**
5. **pdfhttps://www.calstatela.edu/sites/default/files/groups/Department%20of%20Electrical%20and%20Computer%20Engineering/labs/321_manual.pdf**

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

d) Attendance : 5 marks – (Award of marks same as theory subjects)

e) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

f) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C450.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C450.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C450.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C450.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C450.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C450	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**2**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**10**	**3**

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ECC 460 INTEGRATED CIRCUITS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester : 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Integrated Circuits Practical	5	75	25	75	100	3 Hrs

ALLOCATION OF MARKS

CIRCUIT DIAGRAM	: 20
CONNECTION	: 25
EXECUTION & HANDLING OF EQUIPMENT	: 15
OUTPUT / RESULT	: 10
VIVA – VOCE	: 05
TOTAL	**: 75**

COURSE DESCRIPTION:

This is a course on the design and applications of operational amplifiers and analog integrated circuits. This course introduces basic op-amp principles and show how the op-amp can be used to solve a variety of application problems. Much attention is given to basic op-amp configurations, linear and non-linear applications of op-amp and active filter synthesis, including switched capacitor configurations. It also deals with oscillators, waveform generators and data converters.

COURSE OUTCOMES

ECC 460 INTEGRATED CIRCUITS PRACTICAL	
After successful completion of this course, the students should be able to	
C460.1	Infer the truth table of logic gates, Boolean expression,Decoder/Encoder by constructing simple circuits using ICs.
C460.2	Demonstrate the ability to design half adder, full adder, half subtractor , full subtractor that perform the arithmetic operations using IC.
C460.3	Choose the appropriate IC to build Multiplexer, De-multiplexer ,Parity generator and checker, Astable multivibrator.
C460.4	Construct and verify the truth table for RS, D, T & JK, flip-flop & 4- bit ripple counter using IC.
C460.5	Construct a Single digit Decade Counter , DAC and simple power supply using IC.

MAJOR EQUIPMENT REQUIRED:

S.No	Name of the Equipments	Range	Required Nos
1.	IC Trainer Kit	-	06
2.	Function Generator	-	02
3.	Power Supply	(0-30V)	02
4.	CRO	20MHZ	02

OBJECTIVES

- To discuss about ICS and their advantages
- To study basic opamp and its characteristics
- To understand linear circuits using opamp
- To teach linear applications of opamp
- To know about PLL & its applications
- To teach the theory of DAC and its types
- To teach the theory of ADC and its types
- To introduce special function IC – 555 timer
- To study about applications of IC 555
- To learn about fixed IC voltage regulators
- To understand adjustable voltage regulator using IC

ECC 460 INTEGRATED CIRCUITS PRACTICAL

List of Experiments

Note ; At least 5 experiments should be constructed using breadboard

S.No	Name of the experiment	Course Outcome
1.	Verification of truth table of OR, AND, NOT, NOR, NAND, EX-OR gates.	C460. 1
2.	Realization of basic gates using NAND & NOR gates.	C460. 1
3.	Realization of logic circuit for a given Boolean expression.	C460. 1
4.	Half adder using IC's.	C460. 2
5.	Full adder using IC's.	C460. 2
6.	Half subtractor using IC's.	C460. 2
7.	Full subtractor using IC's.	C460. 2
8.	Construction and verification of truth table for Decoder/Encoder.	C460. 3
9.	Multiplexer using multiplexer IC's.	C460.3
10.	De-multiplexer using multiplexer IC's.	C460.3
11.	Parity generator and checker using parity checker/ generator IC's.	C460.4
12.	Construction and verification of truth table for RS, D, T & JK, flip-flop.	C460.4
13.	4- bit ripple counter using FF	C460. 5
14.	Construct a Single digit Decade Counter with 7 segment display.	C460. 5
15.	Astable multivibrator using IC 555.	C460. 5
16.	DAC using R-2R networ	C460. 5
17.	Construction of simple power supply using IC 78XX.	C460. 5

LEARNING WEBSITES

1. **https://www.mcgill.ca/ece/research/integratedcircuits**
2. **http://www.ee.iitm.ac.in/vlsi/start**
3. **http://www.ece.utexas.edu/research/areas/integrated-circuits-systems**
4. **http://www.imb-cnm.csic.es/index.php/en/research/research-groups/integrated-circuits-and-systems**
5. **https://ece.msu.edu/researchfeature/integrated-circuits-and-systems**

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

g)	Attendance	: 5 marks – (Award of marks same as theory subjects)
h)	Procedure/ observation and tabulation/ Other Practical related work	: 10 marks
i)	Record writing	: 10 marks
	Total	**25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C460.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C460.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C460.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C460.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C460.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C460	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**10**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

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ECC470 LIFE AND EMPLOYABILITY SKILL PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

No. of weeks per semester: 15 weeks

Subject	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Autonomous Examination	Total	
Communication And Life Skills Practical	4	60	25	75	100	3 Hrs

TOPICS AND ALLOCATION OF HOURS:

Sl. No.	Section	No. of Hours
1	Part-A: Communication	30
2	Part-B: Entrepreneurship, project preparation, Productivity, Occupational Safety, Health, Hazard, Quality Tools & Labour Welfare	20
3	Part-C: Environment, Global Warming, Pollution	10
Total		60

RATIONALE:

Against the backdrop of the needs of the Industries, as wells as based on fulfilling the expectations of the Industries, the Diploma Level students have to be trained directly and indirectly in toning up their competency levels. Proficiency in Communication only, equips them with confidence and capacity to cope with the employment. Hence, there is a necessity to focus on these in the curriculum. At the end of the Course, the student is better equipped to express himself in oral and written communication effectively.

COURSE OUTCOME

ECC470 LIFE AND EMPLOYABILITY SKILL PRACTICAL

After successful completion of this course, the students should be able to

C470.1 Demonstrate in both oral and written work a discipline-specific critical facility through convincing and well-supported analysis of related arterial.
C470.2 Show the ability to Express Views & Opinions.
C470.3 Develop and Enhance Employability Skills.
C470.4 Motive the Entrepreneurship Skill and Plan for the Future.
C470.5 Show Life Skills for Effective Managerial Ability.

SPECIFIC INSTRUCTIONAL OBJECTIVES

1. Emphasize and Enhance Speaking Skills
2. Increase Ability to Express Views & Opinions
3. Develop and Enhance Employability Skills
4. Induce Entrepreneurship and Plan for the Future
5. Expose & Induce Life Skills for Effective Managerial Ability

LIFE AND EMPLOYABILITY SKILLS PRACTICAL

SYLLABUS

Unit	Topics	Activity	Hours
I	Communication, Listening Training, Facing Interviews, Behavioural Skills	instant sentence making – say expressions/phrases --self - introduction / another higher official in company – describe/explain product – frame questions based on patterns – make sentences based on patterns	30
II	Entrepreneurship, Project Preparation, Marketing Analysis, Support & Procurement	-- prepare an outline of a project to obtain loan from bank in becoming an entrepreneur – prepare a resume	10
III	Productivity – comparison with developed countries, Quality Tools, Circles, Consciousness, Management, House Keeping	-- search in the website -- prepare a presentation – discuss & interact	05
IV	Occupational Safety, Health Hazard, Accident & Safety, First-Aid, Labour Welfare Legislation, Welfare Acts	-- search in the website -- prepare a presentation – discuss & interact	05
V	Environment, Global Warming, Pollution	--taking down notes / hints – answering questions -- fill in blanks the exact words heard	10

LEARNING STRUCTURE **100 Marks**

-- Focus more on Speaking & Listening Skills

-- Attention less on Reading & Writing Skills

-- Apply the skills in fulfilling the Objectives on Focused Topics

a) Listening	**25 Marks**
1. Deductive Reasoning Skills (taking down notes/hints)	**10**
2. Cognitive Skills (answering questions)	**10**
3. Retention Skills (filling in blanks with exact words heard)	**05**
b) Speaking Extempore/ Prepared	**30 Marks**
1. Personality/Psychological Skills (instant sentence making)	**05**
2. Pleasing & Amiable Skills (say in phrases/expressions)	**05**
3. Assertive Skills (introducing oneself/others)	**05**
4. Expressive Skills (describe/explain things)	**05**
5. Fluency/Compatibility Skills (dialogue)	**05**
6. Leadership/Team Spirit Skills (group discussion)	**05**
c) Writing & Reading	**20 Marks**
1. Creative & Reasoning Skills (frame questions on patterns)	**05**
2. Creative & Composing Skills (make sentences on patterns)	**05**
3. Attitude & Aim Skills (prepare resume)	**05**
4. Entrepreneurship Skills (prepare outline of a project)	**05**
d) Continuous Assessment (Internal Marks)	**25 Marks**
(search, read, write down, speak, listen, interact & discuss)	
1. Cognitive Skills (Google search on focused topics)	
2. Presentation Skills & Interactive Skills (after listening, discuss)	
Note down and present in the Record Note on any 5 topics	**10 Marks**
Other activities recorded in the Record note	**10 Marks**
Attendance	**05 Marks**
INTERNAL MARKS	**25 Marks**
EXTERNAL MARKS AT END EXAMINATION	**75 Marks**

MODEL QUESTION

Time: 3 Hours **Maximum Marks: 75**

A. LISTENING **25 Marks**

1. Listen to the content and take down notes/hints 10
2. Listen to the content and answer the following questions. 10
3. Listen to the content and fill in the blanks the exact words heard. 05

B. SPEAKING **30 Marks**

1. Say in a sentence instantly on hearing the word (5 words, one after another). 05
2. Say any five expressions commonly used in communication. 05
3. Imagine, a consultant has come to your department. Introduce him to your subordinates. 05
4. Explain/describe the product you are about to launch in the market. 05
5. Speak with your immediate boss about the progress you have made. 05
6. Discuss within the group on the topic of focus in the syllabus. 05

C. WRITING & READING **20 Marks**

1. Frame new questions from the pattern given by changing sets of words with your own. 05

a.	When	Do	you	return?
b.	How	Is	his performance?	
c.	Where	Has	the manager	gone ?
d.	What	Is	the progress	today?
e.	Why	Are	the machines	not functioning?

2. Make sentences from the pattern given by changing sets of words with your own. 5 marks

a.	The workers	are	on strike		
b.	The labourers	are paid	well	in this factory	
c.	There	is	a rest room	for the workers	
d.	These	are	the new products	launched	by our company
e.	Almost everyone	come	to the company	on motorbikes	

3. Prepare a resume for the post of Department Manager. 5 marks

4. Prepare an outline of a project to obtain a loan. (Provide headings and subheadings) 5 marks

I. Guidelines for setting the question paper:

A. LISTENING : ONLY TOPICS related to

POLLUTION / ENVIRONMENT /

GLOBAL WARMING are to be taken.

These topics are common for all the three types of evaluation.

B. SPEAKING :

1. WORDS of common usage
2. Fragments – expression of politeness, courtesy, cordiality
3. Introduce yourself as an engineer with designation or
   Introduce the official visiting your company/department
4. Describe/Explain the product/machine/department
5. Dialogue must be with someone in the place of work.
6. Group of six/eight Discuss the focused topic
   prescribed in syllabus

C. WRITING & READING:

1. Provide five different structures. Students are to substitute at least one with some other word/words
2. Provide five different structures. Students are to substitute at least one with some other word/words
3. Provide some post related to industries.
4. Outline of the project (skeleton/structure) Only the various headings and subheadings Content is not needed

II. Guidelines for recording the material on the Focused Topics in the Record note.

Write in the record note, **on any five topics**, from the list of topics given below. **10 Marks**

(5 topics x 10 marks = 50 marks. Thus, the **Average of 5 topics is 10 Marks)**

1. Productivity in Industries – Comparison with developed countries
2. Quality Tools, Quality Circles and Quality Consciousness
3. Effective Management
4. House Keeping in Industries
5. Occupational Safety and Hazard
6. Occupational Accident and First Aid
7. Labour Welfare Legislations
8. Labour Welfare Acts and Rights
9. Entrepreneurship
10. Marketing Analysis, Support and Procurement

LABORATORY REQUIREMENT:

1. An echo-free room
2. Necessary furniture and comfortable chairs
3. A minimum of two Computers with internet access
4. A minimum of two different English dailies
5. A minimum of Three Mikes with and without cords
6. Colour Television (minimum size – 29")
7. DVD/VCD Player with Home Theatre speakers
8. Smart board
9. Projector

Suggested Reading:

1. Production and Operations Management by S.N. Chary, TMH
2. Essentials of Management by Koontz & Weihrich, TMH
3. Modern Production / Operations Management by E.S. Buffa and R.K. Sarin, John Wiley & Sons
4. Production Systems: Planning, Analysis and Control by J.L.Riggs, 3rd ed., Wiley.
5. Productions and Operations Management by A.Muhlemann, J.Oakland and K.Lockyer, Macmillan
6. Operations Research - An Introduction by H.A.Taha, Prentice Hall of India
7. Operations Research by J.K.Sharma, Macmillan
8. Business Correspondence & Report Writing by R.C. Sharma and K.Mohan, TMH
9. How to prepare for Group Discussion & Interview (With Audio Cassette) by Prasad, TMH
10. Spoken English – A self-learning guide to conversation practice (with Cassette)
11. Introduction to Environmental Engineering by Mackenzie, L. Davis and A. David, Cornwell, McgrawHill, 3rd Ed.
12. Environmental Engineering by Peary, Rowe and Tchobanoglous, McgrawHill
13. Total Quality Management – An Introductory Text by Paul James, Prentice Hall
14. Quality Control and Applications by Housen & Ghose
15. Industrial Engineering Management by O.P. Khanna

LEARNING WEBSITES

1.http://www.academia.edu/27323966/Life_Skills_English_Lab_Manual_for_Diploma_3rd_Year_V-SEM
2.https://www.scribd.com/document/313429412/30002-Life-and-Employability-Skill-Practical
3.https://ncver.edu.au/__data/assets/file/0022/9751/employability-skills-development-777.pdf
4.https://getthereprojecteu.files.wordpress.com/2016/09/getthere_handbook_en_edit.pdf
5.https://www.researchgate.net/publication/261911512_Employability_skill_development_in_work-integrated_learning_Barriers_and_best_practice

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

j)	Attendance	: 5 marks – (Award of marks same as theory subjects)
k)	Procedure/ observation and tabulation/ Other Practical related work	: 10 marks
l)	Record writing	: 10 marks
	Total	**25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C470.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**1**	**1**
C470.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**1**	**1**
C470.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**1**	**1**
C470.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**1**	**1**
C470.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**1**	**1**
C470	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**10**	**5**	**5**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**1**	**1**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

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ECC 410 INDUSTRIAL ELECTRONICS
MODEL QUESTION PAPER

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
1.	Draw the symbol for MOSFET	I	U
2.	Mention one method to obtain sine wave output from an inverter.	III	U
3.	Mention the methods to control output voltage in inverters.	III	U
4.	Give any one requirement of inverter	III	U
5.	State any one advantage of McMurray inverter	III	U
6.	Mention one input switching device used in PLC	IV	U
7.	Define choppers	II	R
8.	What is local control unit.?.	V	R

PART-B (5x3=15Marks)
Answer any 5 Questions

S.No		Unit	Bloom's Level
9.	Explain On-Line UPS.	III	U
10.	What are the concepts of DC triggering?	I	U
11.	What is importance of Flywheel diode?	II	U
12.	Explain SMPS with its circuit.	III	R
13.	Give difference between on-line UPS and off-line UPS.	III	An
14.	Explain the Logic functions of PLC.	IV	U
15.	What are the features of DCS?	V	U
16.	What are the basic elements of LCU?	V	U

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	Explain the VI characteristics of SCR.	I	R	10
		(OR)			
	B.	Explain parallel inverter using IGBT with a neat diagram.	I	U	10
18	**A.**	Explain Single phase Fully controlled bridge controller with circuit diagram.	II	U	10
		(OR)			
	B.	Explain Jones Chopper with a neat diagram.	II	U	10
19.	**A.**	Draw and explain the single phase inverter with RL load.	III	U	10
		(OR)			
	B.	With a neat diagram, explain the operation of OFF-LINE UPS.	III	U	10
20.	**A.**	(a).Explain the various logic functions used in PLC	IV	U	5
		(b).Explain the ladder diagram of star-delta starter with neat diagram	IV	U	5
		(OR)			
	B.	Explain union with example.	IV	U	10
21.	**A.**	Explain the architecture of DCS	V	U	10
		(OR)			
	B.	Explain LCU.What are its advantages?	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs) R-Remember, U-Understand , Ap-Apply	Higher Order Thinking Skills (HOTs) An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 420 COMMUNICATION ENGINEERING
MODEL QUESTION PAPER

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
1.	What is an antenna?	I	U
2.	Mention the types of propagation.	I	R
3.	Define modulation.	II	U
4.	Define SSB system.	II	R
5.	What is pulse modulation?	III	U
6.	What is a crossover network?	IV	R
7.	What is DVD?	IV	U
8.	Mention advantages of plasma Display.	V	U

PART-B (5x3=15Marks)
Answer any 5 Questions

S.No		Unit	Bloom's Level
9.	Derive the cut of frequency of LPF filter	I	AP
10.	Explain about parabolic antenna.	I	U
11.	Explain about the amplitude modulation with signal diagram	II	U
12.	Explain about low level AM transmitter with neat diagram.	II	R
13.	Explain about Direct FM Transmitter.	III	U
14.	Explain about generate of PAM.	III	U
15.	Explain about the carbon micro phone	IV	U
16.	Explain about TV transmitter	V	U

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	Explain Broadside array & end fire array antennas with neat diagrams	I	U	10
		(OR)			
	B.	Explain about (1) Filters (2) Attenuators.	I	U	10
18	**A.**	Explain the high level AM transmitter with block diagram	II	U	10
		(OR)			
	B.	Explain the super heterodyne receiver with block diagram.	II	U	10
19.	**A.**	Explain indirect method of FM transmission and Compare FM&AM	III	AP	10
		(OR)			
	B.	Derive the expression for Modulation Index for Frequency Modulation.	III	AP	10
20.	**A.**	Explain construction and working of velocity ribbon microphone	IV	U	10
		(OR)			
	B.	Explain in detail about CD recording and reproduction.	IV	U	10
21.	**A.**	Explain the composite video signal with diagram	V	U	10
		(OR)			
	B.	Give brief notes on 1.Plasma display 2. Handycam	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 430 DIGITAL ELECTRONICS
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
1.	Convert (175)8 into decimal.	I	R
2.	Write the truth table for AND Gate.	I	R
3.	Write the application of multiplexer.	I	U
4.	What are the weights of hexadecimal and decimal numbers?	II	R
5.	What is encoder?	I	R
6.	Define flip-flop.	III	R
7.	Mention the types of flip-flops.	III	R
8.	Write about Opcode fetch.	V	R

PART-B (5x3=15Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
9.	Construct OR, AND, NAND gates by using only NOR gates.	I	U
10.	Write about full adder.	II	U
11.	Explain BCD to seven segment decoder.	II	U
12.	Write about mod 3 counter.	II	U
13.	Write about T - Flip flop.	III	U
14.	Write about dynamic RAM.	IV	U
15.	Explain flash memory.	IV	U
16.	What are various addressing mode?	V	R

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	Simplify the given logic function using Karnaugh map and simulated its output. $F = \sum (0,2,4,6,8,10,12,14)$	I	E	10
		(OR)			
	B.	Simplification of expression using Boolean techniques	I	U	10
18	**A.**	Explain the operation of BCD adder with neat diagram.	II	U	10
		(OR)			
	B.	Explain 4 to 1 MUX, 8 to 1 MUX and applications of the MUX.	II	U	10
19.	**A.**	Explain Mod 3, Mod 7 counter.	III	U	10
		(OR)			
	B.	Explain Serial IN Serial OUT- Serial IN Parallel OUT	III	U	10
20.	**A.**	Explain Classification of memories.	IV	U	10
		(OR)			
	B.	Explain PROM- EPROM- and EEPROM	IV	U	10
21.	**A.**	Explain Memory mapped I/O and I/O mapped I/O and its Comparison	V	An	10
		(OR)			
	B.	Explain memory read- memory write- I/O read, I/O write	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs) R-Remember, U-Understand , Ap-Apply	Higher Order Thinking Skills (HOTs) An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECC 440 LINEAR INTEGRATED CIRCUITS

MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
1.	What is Op amp?	I	R
2.	Define Slew rate.	I	U
3.	What is Voltage follower?	II	R
4.	What is multiplier?	II	R
5.	What is VCO?	III	R
6.	What is PLL?	III	R
7.	Mention types of DAC.	IV	U
8.	What is IC LM723?	V	R

PART-B (5x3=15Marks)
Answer any 5 Questions

S.No		Unit	Bloom's Level
9.	Draw the Block diagram of op-amp.	I	U
10.	Draw the equivalent circuit of an op-amp.	I	U
11.	Explain the op-amp used as summing amplifier.	II	AP
12.	Explain voltage to current converter using op-amp.	II	AP
13.	Explain the operation of PLL.	III	U
14.	Explain the operation of VCO.	I	U
15.	Explain sampling.	IV	U
16.	Draw the block diagram of monostable multivibrator using IC 555.	V	AP

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	With a neat diagram explain inverting and non-inverting amplifier using op-amp.	I	AP	10
		(OR)			
	B.	Explain Scale changer using op-amp.	I	AP	10
18	**A.**	Explain zero crossing detector.	II	U	10
		(OR)			
	B.	With a neat diagram explain the operation of saw tooth generator using op-amp.	II	AP	10
19.	**A.**	Draw the block diagram and explain the Operation of PLL	III	U	10
		(OR)			
	B.	Draw and Explain the VCO 566	III	U	10
20.	**A.**	Explain the Operation of R-2R Ladder D/A Converter	IV	U	10
		(OR)			
	B.	Explain the Functional Block diagram of IC ADC 0808	IV	U	10
21.	**A.**	Explain the functional Block diagram of IC555 and its Applications.	V	U	10
		(OR)			
	B.	Explain the Low voltage and High voltage regulator using LM 723.	V	AP	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECC 510 ADVANCED COMMUNICATION SYSTEMS

TEACHING AND SCHEME OFEXAMINATION:

Number of Weeks/ Semester : 15 Weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Weeks	Hrs/ Semester	Internal Assessment	Semester End Examination	Total	
Advanced Communication Systems	5	75	25	75	100	3Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME(Hrs)
I	Radar, Navigational Aids, Telephony and fax, facsimile communication system	13
II	Digital Communication and Digital codes	13
III	Optical Communication	12
IV	Satellite Communication & Microwave Communication	13
V	Mobile Communication &Satellite multiple access technique	12
Revision & Test		12
Total		**75**

Course Description:

The introduction of this subject will enable the students to learn about the advancement in communication systems. It will give exposure to the various modes of communication viz Radar, Telephone, Fax, digital communication, digital codes, fiber optical communication, satellite communication, microwave communication, mobile communication and Satellite multiple access techniques.

Objectives

- To understand principles of Radar
- To understand principles of navigational aids
- To study Electronic Exchange and principles of facsimile communication
- To study basic digital communication system and digital codes.
- To learn Error detection and correction codes and various digital modulation techniques.
- To understand optical communication system and discuss about fiber mode, configurations, losses.
- To learn optical sources, optical detectors.

- To discuss the applications of fiber optic communication
- To Study satellite system, orbits, launching, Antennas
- To study about satellite services
- To understand fundamentals of Microwave communication
- To study fundamental cellular concepts such as frequency reuse, handoff
- To learn multiple access techniques.
- To learn digital cellular system – GSM

COURSE OUTCOMES

ECC 510 ADVANCED COMMUNICATION SYSTEMS

After successful completion of this course, the students should be able to

C510.1 Explain the fundamentals of RADAR, display methods, its applications and Telephony and Facsimile.

C510.2 Interpret about Digital communication systems

C510.3 Explain about Optical communication systems

C510.4 Show the knowledge on Satellite communication and Microwave communication systems

C510.5 Explain about cellular Mobile communication.

ECC 510 ADVANCED COMMUNICATION SYSTEMS

UNIT I

RADAR AND NAVIGATIONAL AIDS: **[13 Hrs]**

Basic Radar System– Applications [1 Hr]

Radar range equation (qualitative treatment only)

Factors influencing maximum range [1 Hr]

Basic Pulse Radar System – Block Diagram [2 Hrs]

Display Methods A - Scope, PPI Display

Instrument landing system – Ground controlled approach system [2 Hrs]

TELEPHONY AND FAX:

Telephone system–Public Switched Telephone Network (PSTN) [2 Hrs]

Electronic Switching System - Block diagram

ISDN – Architecture, Features - Video phone – Block diagram [2 Hrs]

FACSIMILE COMMUNICATION SYSTEM:

Facsimile Sender-Cylindrical Scanning- Facsimile receiver [3 Hrs]

Synchronization-Phasing – Index of Cooperation (IOC) – Direct Recording.

UNIT-II

DIGITAL COMMUNICATION: **[13 Hrs]**

Basic Elements of digital communication system – block diagram [2 Hrs]

Characteristics of data transmission circuits

Bandwidth requirement- speed - Baud rate, Noise, Cross talk, Distortion [1 Hr]

Digital codes – ASCII Code – EBCDIC Code [2 Hrs]

Error detection codes – Parity check codes

Redundant codes - Error correction codes – Retransmission [1 Hr]

Forward error correcting code- hamming Code [3 Hrs]

Digital modulation techniques – ASK, FSK, PSK [2 Hrs]

QPSK modulation/demodulation techniques [2 Hrs]

(only block diagram and operation).

UNIT-III

OPTICAL COMMUNICATION: **[12 Hrs]**

Optical Communication System– Block diagram [2 Hrs]

Advantages of optical fiber Communication systems

Principles of light transmission in a fiber using Ray Theory [2 Hrs]

Single mode fibers, multimode fibers

Step index fibers, graded index fibers (basic concepts only) [2 Hrs]

Attenuation in optical fibers – Absorption losses

Scattering losses, bending losses, core and cladding losses [2 Hrs]

Optical sources – LED - semiconductor LASER – Principles

Optical detectors – PIN and APD diodes [2 Hrs]

Connectors - Splices – Couplers

Optical transmitter – Block diagram – optical receiver Block diagram [2 Hrs]

Application of optical fibers – Networking, Industry and Military applications.

WDM – OTDR (Block diagram and Explanation only)

UNIT-IV

SATELLITE COMMUNICATION: **[13 Hrs]**

Satellite system: Kepler's I,II,III laws – orbits – launching orbits - types [2 Hrs]

Geostationary synchronous satellites- Advantage

Apogee -Perigee- Active and passive satellite - Earth eclipse of satellite

Antenna: Parabolic reflector antenna - cassegrain antenna - Space segment [2 Hrs]

power supply- Attitude control [1Hr]

station keeping - Transponders – TT and C subsystem - Antenna Subsystem [1Hr]

Earth segment—Block diagram of Transmit receive earth station [2 Hrs]

Satellite mobile services - Basics of GPS

MICROWAVE COMMUNICATION:

Microwave frequency ranges [2 Hrs]

Microwave devices – Parametric amplifiers

Travelling wave tubes –simple block diagram of microwave transmitter, [2 Hrs]

receiver and microwave link repeater.

Reflex Klystron – Magnetron - TWT [1Hr]

UNIT-V

MOBILE COMMUNICATION: (Qualitative Treatment only) **[12 Hrs]**

Cellular telephone– fundamental concepts – Simplified Cellular telephone system [2 Hrs]
frequency reuse – Interference – Co-Channel Interference
Adjacent Channel Interference – Improving coverage and [2 Hrs]
capacity in cellular systems
cell splitting – sectoring - Roaming and Handoff – [2 Hrs]
Basics of Bluetooth technology
Satellite multiple access techniques [2 Hrs]
TDMA, FDMA, CDMA
Digital cellular system – Global system for mobile communications (GSM) [2 Hrs]
GSM services – GSM System Architecture - Basics of GPRS. [2 Hrs]

Revision and Test **[12 Hrs]**

TEXT BOOK:

Sl. No	Title	Author	Publisher with Edition
1.	Electronic Communication Systems	Wayne H.Schiller	Pearson Education – Second Edition, 2005
2.	Optical communication	John Gower	PHI Second Edition – 1995
3.	Wireless Communication	Theodore S.Rappaort	Pearson Education Second Edition, 2002

REFERENCE BOOKS:

Sl. No	Title	Author	Publisher with Edition
1.	Electronic Communication Systems	Kennedy – Davis	Tata McGraw Hill, Fourth Edition, 1999
2.	Electronics Communication	Dennis Roddy - John coolen	PHI, Third Edition, 1988
3.	Optical Fiber Communication	Gerd Keiser	McGraw Hill, Third Edition, 2000
4.	Satellite Communication	Dr. D.C.Agarwal	Khanna Publishers, Third Edition, 2006
5.	Electronic Communications Systems(Fundamentals through Advanced)	Wayne Tomasi	Pearson Education , Fifth Edition, 2005

LEARNING WEBSITES

1.https://lecturenotes.in/subject/74/advanced-communication-system-acs

2.http://www.juit.ac.in/jcourses/pdf/10M11EC111.pdf

3. https://www.linkedin.com/company/advanced-communication-solutions-inc-

4. https://www.nasa.gov/pdf/203071main_Advanced%20Communications%20-

5. http://www.advcommsystems.com/

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	-	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
C510.1	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**2**	**3**	**2**
C510.2	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**2**	**3**	**2**
C510.3	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**2**	**3**	**2**
C510.4	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**2**	**3**	**2**
C510.5	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**2**	**3**	**2**
C510	**15**	**10**	**10**	**10**	**10**	**10**	**15**	**10**	**15**	**10**
Correlation Level	**3**	**2**	**2**	**2**	**2**	**2**	**3**	**2**	**3**	**2**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 520 MICROCONTROLLER

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs / Semester	Internal Assessment	SEMESTER end Examination	Total	
Microcontroller	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME (Hrs)
I	Architecture & Instruction set of 8051	13
II	Programming Examples	13
III	I/O and Timer	13
IV	Interrupt and Serial Communication	12
V	Interfacing Techniques.	12
	Revision Test	12
	TOTAL	**75**

COURSE DESCRIPTION

The 8051 Microcontroller is one of the most popular general purpose microcontrollers especially designed for embedded systems. The first version of this single chip microcontroller came in 1980s, and since then it has been being used for embedded systems especially in robotics. It a small chip based on an architecture with support for embedded applications, such as measuring device, security systems, robotics, remote control applications, scroll message display, etc.

Objectives:

On completion of the following units of syllabus contents, the students must be able to

- Understand the architecture of 8051 Microcontroller.
- Understand the functions of various registers.
- Understand interrupt structure of 8051.
- Understand serial data communication concepts.
- Understand the programming techniques.
- Know various addressing modes.
- Write simpler programs using 8051.
- Understand the block diagram and control word formats for peripheral devices.
- Understand how to interface with RS232C.
- Understand how to interface with 8255.
- Understand various application of 8051 Microcontroller.

COURSE OUTCOMES

ECC 520 MICROCONTROLLER

After successful completion of this course, the students should be able to

C520.1 Tell the fundamentals of microcontroller 8051, addressing modes, memory, interrupts, counter ,registers and instruction sets.

C520.2 Analyze the assembler and addressing modes of 8051 microcontroller and write assembly language program for microcontroller.

C520.3 Develop I/O programming, modes of Timer and Counter programming.

C520.4 Build 8051 Serial Communication Programming, Programming Timer Interrupts and Programming the Serial Communication Interrupt.

C520.5 Explain the importance of different peripheral devices and their interfacing to microcontrollers.

ECC 520 MICROCONTROLLER

UNIT – I

ARCHITECTURE & INSTRUCTION SET OF 8051: **[13Hrs]**

Comparison of Microprocessor and Microcontroller [2 Hrs]

Block diagram of Microcontroller – Functions of each block –

Pin details of 8051 [1 Hr]

ALU – ROM – RAM – Memory Organization of 8051

Special function registers – Program Counter – PSW register [2 Hrs]

Stack - I/O Ports – Timer – Interrupt – Serial Port [1 Hr]

Oscillator and Clock – Clock Cycle – State - Machine Cycle – Instruction cycle [2 Hrs]

Reset – Power on Reset – Overview of 8051 Family

Instruction set of 8051 – Classification of 8051 Instructions [2 Hrs]

Data transfer Instructions – Arithmetic Instructions – Logical Instructions [2 Hrs]

Branching Instructions – Bit Manipulation Instructions. [1 Hr]

UNIT – II

PROGRAMMING EXAMPLES: **[13 Hrs]**

Assembler and addressing modes

Assembling and running an 8051 program [1 Hr]

Structure of Assembly Language – Assembler directives [1 Hr]

Different addressing modes of 8051 – Programmes – Multibyte Addition [2 Hrs]

8 Bit Multiplication and Division [1 Hr]

Biggest Number / Smallest Number – Ascending order / Descending order [2 Hrs]

BCD to HEX Conversion – HEX to BCD Conversion [2 Hrs]

BCD to ASCII Conversion – ASCII to Binary Conversion [2 Hrs]

Odd Parity Generator - even Parity Generator – Time delay routines. [2 Hrs]

UNIT – III

I/O AND TIMER: **[13 Hrs]**

Bit addresses for I/O and RAM – I/O programming [1 Hr]

I/O bit manipulation programming [2 Hrs]

Programming 8051 Timers – Timer 0 and Timer 1 registers [3 Hrs]

Different modes of Timer – Mode 0 Programming – Mode 1 Programming

Mode 2 Programming [2Hrs]

Counter programming – Different modes of Counter [1 Hr]

Mode 0 Programming – Mode 1 Programming [2 Hrs]

Mode 2 Programming – (simple programs). [2Hrs]

UNIT – IV

INTERRUPT AND SERIAL COMMUNICATION: [12 Hrs]

SERIAL COMMUNICATION

Basics of Serial programming [1 Hr]

RS 232 Standards – 8051 connection to RS 232 [2 Hrs]

8051 Serial Communication Programming [2 Hrs]

Programming 8051 to transmit data serially –

Programming 8051 to Receive data serially [2 Hrs]

8051 Interrupts – Programming Timer Interrupts [2 Hrs]

Programming External Hardware Interrupts –

Programming the Serial Communication Interrupt [2Hrs]

Interrupt Priority in 8051 (simple Programs) [1 Hrs]

UNIT – V

INTERFACING TECHNIQUES: [12 Hrs]

IC 8255

IC 8255 – Block Diagram – Modes of 8255 [2 Hrs]

INTERFACING TECHNIQUES

Interfacing External Memory to 8051 – 8051 Interfacing with the 8255 [2 Hrs]

ASM Programming [1 Hrs]

Relays – Sensor Interfacing [2 Hrs]

ADC Interfacing – DAC Interfacing [2 Hrs]

Keyboard Interfacing – Seven segment LED Display Interfacing [2 Hrs]

Stepper Motor Interfacing – DC Motor Interfacing using PWM [1 Hrs]

Revision and Test [12 Hrs]

TEXT BOOKS:

Si.No	Title	Author	Publisher with Edition
1.	Microcontrollers, Principles and Applications	Ajit pal	PHI Ltd., - 2011
2.	Microprocessor and Microcontroller	A.P.Godse & D.A.Godse	Technical Publication., - 2011.

REFERENCE BOOKS:

Si.No	Title	Author	Publisher with Edition
1.	8051 Microcontroller and Embedded Systems using Assembly and C	Mazidi, Mazidi and D.MacKinlay	2006 Pearson Education Low Price Edition

2.	Microprocessor and Microcontroller	R.Theagarajan	Sci Tech Publication, Chennai - 2000
3.	8051 Microcontroller	Kenneth J.Ayala.	Tata MCGraw Hill - 1994
4.	Programming & Customizing the 8051 Microcontroller	Myke Predko	TATA McGraw – Hill Publication,edition – 1994.
5.	Microprocessor and Microcontroller	B.P.Singh, Galgotia Publication Pvt.Ltd	PHI Ltd., First edition 1994.

LEARNING WEBSITES

1. https://www.elprocus.com/8051-microcontroller-architecture-and-applications/
2. https://www.tutorialspoint.com/microprocessor/microcontrollers_8051_architecture.htm
3. https://www.electronicshub.org/8051-microcontroller-introduction/
4. http://www.circuitstoday.com/8051-microcontroller
5. https://www.engineersgarage.com/what-is-8051-microcontroller

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
C520.1	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**3**	**2**	**2**
C520.2	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**3**	**2**	**2**
C520.3	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**3**	**2**	**2**
C520.4	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**3**	**2**	**2**
C520.5	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**3**	**2**	**2**
C520	**15**	**10**	**10**	**10**	**15**	**10**	**15**	**15**	**10**	**10**
Correlation Level	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**3**	**2**	**2**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs) R-Remember, U-Understand , Ap-Apply	Higher Order Thinking Skills (HOTs) An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 530 VERY LARGE SCALE INTEGRATION
(ELECTIVE – I)

SCHEME OF INSTRUCTION AND EXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Very Large Scale Integration	6	90	25	75	100	3 Hrs

TOPICS AND ALLOCATIONS

UNIT	TOPIC	TIME (hrs)
I	Combinational Logical Circuits	16
II	VHDL for Combinational logic circuit	16
III	Sequential Logic circuits	16
IV	VHDL for sequential Logic circuits	15
V	PLDS and FPGA circuits	15
	Revision, Test	12
	TOTAL	**90**

COURSE DESCRIPTION

Very Large Scale integration technology, when especially used for digital integrated circuit design, is that it is mandatory the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware fabrication in the foundry (gates and wires). Hardware Description Language (HDL) allows designs to be described using any methodology - top down, bottom up or middle out! VHDL can be used to describe hardware at the gate level or in a more abstract way. This course is to introduce the digital system design concepts through hardware description Language, VHDL programming, design flow of VLSI, and architectures of CPLD and FPGA. It is mainly aimed at design of combinational and sequential functions at gate / behavioral level and simulates and verifies their functionality using the Hardware description Language (VHDL).

OBJECTIVES

On successful completion of the course the students must be able to

- Understand device level implementation of digital gates.
- Understand the combinational circuit design and optimizing of the gate
- Design a combinational circuit for any custom made application
- Explain the building blocks for the combinational circuit
- Understand the VHDL code and circuit design process.
- Develop a VHDL code for any combinational circuit
- Answer the VHDL primitives and the importance of VHDL code in a digital circuit
- Design a digital circuit with Muxes and Encoders
- Understand the functionality of various flipflops through its excitation table.
- Design of a sequential circuit for any custom made application
- Explain the style of moore and mealy type machines
- Understand to implement VHDL code for various flipflops
- Design of sequential circuit and implementation with VHDL code
- Explain the importance of PROM, PLA, PAL and PLD
- Differentiate between the PROM,PLA and PAL.
- Develop the circuit using PROM,PAL and PLA.
- Understand the CPLD and FPGA hardware.
- Describe ASICs

COURSE OUTCOMES

ECC 530 VERY LARGE SCALE INTEGRATION

After successful completion of this course, the students should be able to

C530.1 Explain the combinational circuit design and building blocks.
C530.2 Develop VHDL codes for logic circuits.
C530.3 Analyze the sequential circuit design.
C530.4 Develop VHDL codes for Sequential Circuits
C530.5 Distinguish between PLDs and FPGA

ECC 530 VERY LARGE SCALE INTEGRATION
(ELECTIVE – I)

UNIT – I	**[16 HRS]**
COMBINATIONAL CIRCUIT DESIGN: NMOS and CMOS logic	[3 Hrs]
implementation of Switch, NOT, AND, OR, NAND, and NOR gates-	
CMOS transmission gates- NMOS & CMOS Fabrication Process Sequence	[2 Hrs]
Digital logic variable, functions, inversion, gate/circuits,	
Boolean algebra and circuit synthesis using gates (Up to 4 variables).	[3 Hrs]
COMBINATIONAL CIRCUIT BUILDING BLOCKS:	
Circuit synthesis using Multiplexer, Demultiplexer, Encoders and Decoders.	[2 Hrs]
Arithmetic adder, Subtractor and Comparator circuits.	[3 Hrs]
Hazards and races	[3 Hrs]
UNIT – II	**[16 HRS]**
VHDL FOR COMBINATIONAL CIRCUIT:	
Introduction to VLSI and its design process	[3 Hrs]
Introduction to CAD tool and VHDL: Design Entry, Synthesis, and Simulation.	[3 Hrs]
Introduction to HDL and different level of abstraction VHDL	
Statements and Assignment,	[3 Hrs]
VHDL CODE: AND, OR, NAND, NOR gates, Implementation of	[4 Hrs]
Mux, Demux, Encoder, decoder.	
Four bit Arithmetic adder, subtractor and comparator in VHDL	[3 Hrs]
UNIT - III	**[16 HRS]**
SEQUENTIAL CIRCUIT DESIGN: Introduction/Refreshing to	[3 Hrs]
Flip-flops and its excitation table, counters and Shift registers.	
DESIGN STEPS: State diagram, State table, and state assignment.	[3 Hrs]
Example for moore and mealy machines.	[3 Hrs]
Design of modulo counter	[2 Hrs]
(upto 3 bit) with only D flip-flops through state diagram	[3Hrs]
JK flip-flops through state diagram	[2 Hrs]

UNIT - IV **[15 HRS]**

VHDL FOR SEQUENTIAL CIRCUIT:

VHDL constructs for storage elements [3 Hrs]

VHDL code for D Latch / D, JK and [3 Hrs]

T Flip-flops with or without reset input. [2 Hrs]

VHDL EXAMPLES: Counters: Synchronous counters-2 bit &3 bit up counter. [2 Hrs]

3 bit up/down counter Decade counter, Johnson Counter [3 Hrs]

VHDL code for serial Adder [2 Hrs]

UNIT - V

PLDS AND FPGA **[15 HRS]**

Introduction to PROM, PLA and PAL. Implementation of [3 Hrs]

combinational circuits with PROM,,PAL and PLA (upto 4 variable).

Comparision between PROM, PLA and PAL [3 Hrs]

Introduction to Complex Programmable Logic device [3 Hrs]

Field Programmable Gate Array [3 Hrs]

Introduction to ASIC, Types of ASIC [3 Hrs]

Revision and Test **[12 Hrs]**

TEXT BOOKS:

SL.No	Title	Author	Publisher with Edition
1.	"Digital Design"	M.Morris Mano Michael D Ciletti	Pearson Education, 2008
2.	"Fundamentals of Digital Logic with VHDL design"	Stephen brown and Vranesic	Tata McGraw Hill, Second edition, 2008
3.	" VHDL Primer"	Bhasker J	Prentice Hall India, 2009

REFERENCE BOOKS :

SL.No	Title	Author	Publisher with Edition
1.	"Digital Electronics with PLD Integration"	Nigel P. Cook	Prentice Hall, 2000
2.	"Programmable Logic Handbook: PLD, CPLD, and FPGA"	Ashok K.Sharma,	Mcgraw-Hill, 1998
3.	Digital Logic Simulation and CPLD Programming with VHDL"	Steve Waterman	Prentice Hall, 2002
4.	VHDL Design Representation and synthesis	James R.Armstrong F.Gail gray	Pearson Education, 2nd Edition, 2001
5.	VHDL Programming by Example	Douglas L.Perry	TATA McGraw Hill, 3rd Edition, 2003

LEARNING WEBSITES

1.https://www.techopedia.com/definition/714/very-large-scale-integration-vlsi

2.https://electronicsforu.com/resources/learn-electronics/vlsi-developments-ic-fabrication

3.http://ece-research.unm.edu/jimp/vlsi/slides/c1_intro.html

4.https://www.engineersgarage.com/articles/vlsi-design-future

5.https://en.wikipedia.org/ wiki/VLSI_Technology

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C530.1	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C530.2	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C530.3	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C530.4	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C530.5	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C530	**15**	**10**	**10**	**10**	**15**	**10**	**15**	**10**	**15**	**15**
Correlation Level	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**

Correlation level 1 – Slight (low)

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QUESTION PAPER SETTING

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% to be included	R-Remember, U-Understand , Ap-Apply 90%	An-Analyze, E-Evaluate, C-Create 10%

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ECC 541 DIGITAL COMMUNICATION

TEACHING AND SCHEME OFEXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
Digital Communication	Hrs week	Hrs semester	Marks			Duration
			Internal assessment	Semester End Examination	Total	
	5	75	25	75	100	3Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME(Hrs)
I	Basics of digital communication	13
II	Formatting and Base Band Modulation	13
III	Baseband Coding Techniques	13
IV	Digital Modulation Techniques	12
V	Spread Spectrum Techniques	12
Revision Test		12
Total		**75**

Course description:

Today, the growth of any industry depends upon electronics and communication. There is the need for digital techniques in each and every field. The reason behind the introduction of this subject is to impart technical excel hence in the field of digital communication by analyzing the various digital transmission methods, error control methods modulation , Baseband modulation, Baseband coding techniques and Spread Spectrum Techniques.

OBJECTIVES:

- To know the Basics of Digital Communication
- To study about the various types of signals
- To study about the data transmission
- To understand the Baseband system and sampling
- To learn about PCM waveform types
- To study about M-ary pulse modulation
- To learn about rationale for coding
- To learn about types of coding methods

- To study about various error control codes
- To know the Digital modulation techniques
- To learn about TDM frame structure
- To study about coherent detection of PSK, FSK
- To understand the Spread spectrum communication
- To study the Jamming consideration
- To study about CDMA Digital cellular system

COURSE OUTCOMES

ECC 541 DIGITAL COMMUNICATION

After successful completion of this course, the students should be able to

C 541 .1 Explain the basics of Digital Communication

C 541 .2 Interpret about formatting and base band transmission.

C 541 .3 Analyse about base band coding techniques.

C 541 .4 Define different digital modulation techniques.

C 541 .5 Interpret about Spread Spectrum Techniques.

ECC 541 DIGITAL COMMUNICATION

UNIT I

BASICS OF DIGITAL COMMUNICATION **[13 Hrs]**

Digital communication signal Processing – Typical Block diagram of transformations [2 Hrs]

Advantages over analog communication – Channels for Digital communication [2 Hrs]

Telephone, Optical fiber, Satellite [2 Hrs]

Classification of signals – deterministic and random signals – Periodic and non periodic signals – analog and discrete signals – energy and power signals – unit impulse function [2 Hrs]

Information capacity (Definition only) – Shannon's limit for information capacity (Definition only) [2 Hrs]

Data transmission [1 Hr]

Serial and parallel transmission -Synchronous and asynchronous transmission [2 Hrs]

UNIT II

FORMATTING AND BASEBAND MODULATION **[13 Hrs]**

Base band system – The Sampling theorem – impulse sampling – [2 Hrs]

natural sampling - Sample and hold operation – spectra [1 Hr]

Nyquist theorem – aliasing – signal interface for a digital system – Sampling and quantizing effects- Quantization noise [2 Hrs]

channel effects – channel noise - PCM – uniform and Non-uniform quantization [2 Hrs]

Baseband Transmission:

PCM waveform types – non return-to-zero(NRZ) - return-to-zero(RZ) [2 Hrs]

Phase encoded – multilevel binary – special attributes of PCM waveforms [2 Hrs]

Bits per PCM word and Bits per symbol – PCM per size [2 Hrs]

M-ary pulse modulation Waveforms

UNIT III

BASEBAND CODING TECHNIQUES: **[13 Hrs]**

Rationale for coding – Types of codes – Discrete memoryless channel [2 Hrs]

Error control coding methods - Forward error correction [2 Hrs]

Error detection with retransmission – types of error [2 Hrs]

Random error and burst error [2 Hrs]

Principles of linear block codes – Hamming code [3 Hrs]

Binary cyclic codes - Cyclic redundancy check code(CRC) [2 Hrs]

Convolution code

UNIT IV

DIGITAL MODULATION TECHNIQUES: **[12 Hrs]**

Digital modulation techniques – Listing of various types [2 Hrs]

Coherent binary modulation techniques - Coherent quadrature modulation techniques – Non-Coherent binary modulation techniques [3 Hrs]

Minimum shift keying (MSK) – Block diagram of MSK transmitter and receiver [2 Hrs]

TDM – Frame structure, ASCII Framing

E1 Framing – T1 framing for telephone [2 Hrs]

Detection of signals – coherent detection of PSK – sampled matched filter

Coherent detection of FSK – Non-coherent detection – Binary differential PSK [3 Hrs]

UNIT V

SPREAD SPECTRUM TECHNIQUES : **[12 Hrs]**

Spread spectrum Communication – Beneficial attributes of Spread spectrum systems - Pseudo noise sequences [3 Hrs]

Randomness properties – Balance property, Run property and correlation property [2 Hrs]

Direct sequence spread spectrum systems – Processing gain and performance [2 Hrs]

Frequency hopping systems – Frequency hopping with diversity [2 Hrs]

Fast hopping versus – slow hopping – Synchronization – Jamming consideration [2 Hrs]

Commercial application – CDMA digital cellular system [1 Hr]

Revision and Test **[12 Hrs]**

TEXT BOOKS:

Sl. No	Title	Author	Publisher with Edition
1.	Digital Communication	Simon Haykins	Wiley India edition, 2006
2.	Principles of Digital communication	J.S.Chitode	Tech Publications, Pune, Second edition,2011

REFERENCE BOOKS:

Sl.No	Title	Author	Publisher with Edition
1.	Digital communications Fundamentals & Applications	Bernard Sklar & Pabitra Kumar Ray	Pearson, Second edition, 2009
2.	Digital and analog communication system	B.P.Lathi .Zhi Ding	OXFORD university press. International 4th Edition - 2001
3.	Digital Communication	P.Ramakrishna Rao	TMH, 2011
4.	Principles of Communications system	Taub &Schilling	TMH, Third edition, 2008
5.	Digital communications	John G.Prokais	TMH 2011
6.	Digital communications	Dr.K.N.Hari Bhat Dr.D.Ganesh Rao	Sanguine Technical Publisher 2005

Learning websites

1.https://nptel.ac.in/courses/Webcourse-contents/IISc-BANG/Data%20Communication/Learning%20Material%20-%20DataCommunication.pdf

2.https://www.slideshare.net/lineking/digital-communication-system

3.https://www.sciencedirect.com/topics/engineering/digital-communication-system

4.https://www.allaboutcircuits.com/textbook/digital/chpt-14/introduction-to-digital-communication/

5.https://www.tutorialspoint.com/digital_communication/digital_communication_quick_guide.htm

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PSO1**	**PSO2**	**PSO3**
C541.1	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C541.2	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C541.3	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C541.4	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C541.5	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C541	**15**	**10**	**10**	**10**	**15**	**10**	**15**	**10**	**15**	**10**
Correlation Level	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
% to be included	R-Remember, U-Understand , Ap-Apply 90%	An-Analyze, E-Evaluate, C-Create 10%

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ECC 542 PROGRAMMABLE LOGIC CONTROLLERS

TEACHING AND SCHEME OFEXAMINATION:

Number of weeks per Semester: 15 weeks

Course	Instruction		Examination			
Programmable Logic Controllers	**Hrs/ week**	**Hrs/ semester**	**Marks**			**Duration**
			Internal assessment	**Semester End Examination**	**Total**	
	5	75	25	75	100	3Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME(Hrs)
I	Architecture and operation of PLC	13
II	Programming of PLC	13
III	PLC Timers and counters	13
IV	Advanced instructions	12
V	I/O Module Communication and networking	12
Revision and Test		12
Total		**75**

COURSE DESCRIPTION

Programmable Logic Controller is the mandatory for the control Engineers in any Process Industry. As it is the default controller being used in the industries in automation of process such as packing, discrete control etc., It is obvious for the instrumentation and control Engineer to understand Hardware and programming the PLC.

Objectives

- To understand the detailed Hardware of PLC and its parts
- To understand the working of PLC and scan cycle
- T o understand the program and data memory organization
- To know the Different timers of PLC and programming them
- To know the different counters of PLC and its parameters
- To understand the Ladder logic programming of PLC
- To develop simple ladder programs
- To study the Advanced instructions of PLC
- To understand the communication module of PLC

COURSE OUTCOMES

ECC 542 PROGRAMMABLE LOGIC CONTROLLERS	
C 542 .1	Explain the architecture and operation of PLC.
C 542 .2	Develop the programming of PLC.
C 542 .3	Interpret the concepts PLC timers and counters.
C 542 .4	Recall the advanced instructions in PLC.
C 542 .5	Explain I/O module communication and networking

ECC 542 PROGRAMMABLE LOGIC CONTROLLERS

UNIT I

ARCHITECTURE AND OPERATION OF PLC **[13 HRS]**

Evolution of PLCs – Hard – Wired control systems [2 Hrs]

PLC definition, Features, Advantages, Relays

PLC parts and architecture – CPU - I/O section – Programming device [1 Hr]

Memory - input field devices –output field devices – input module wiring [2 Hrs]
connections, output module wiring connections

Power supply – PLC versus computer – Types of PLC [2 Hrs]

Single ended – Multitask – Control management – unitary [2 Hrs]

Modular – small – medium – large

Developing circuits from Boolean expressions – [2 Hrs]

Hardwired logic to programmed logic

Programming word level logic instruction – Processor memory organization [2 Hrs]

program files – Data files – Program Scan

UNIT II

PROGRAMMING OF PLC **[13 Hrs]**

PLC programming languages – Standard languages – Ladder diagram(LD) [2 Hrs]

Function block diagram(FBD) – Sequential function chart(SFC) [2 Hrs]

Statement list(STL) (each one example program)

Symbols of a PLC input and output contact graphical languages(IES) – [2 Hrs]

program format – Typical numbering mode

Equivalent ladder diagram of AND,OR,NOT,XOR,NAND and NOR [3 Hrs]

gate equivalent ladder diagram to demonstrates De-morgan's theorem

Ladder design switches – Develop elementary [2 Hrs]

Program design of a 4:1 multiplexer using ladder logic programming [2 Hrs]

wired level logic instructions input, output, flag, timer, counter, latch

UNIT III

PLC TIMERS AND COUNTERS **[13 HRS]**

Definition and classification of a timer – Characteristics of a PLC timer [2 Hrs]

Functions in a timer - resetting – retentive functions and
function block format – non retentive [3 Hrs]

Classification – Timer ON–delay – timer – OFF delay
Simple problems using timer [2 Hrs]

PLC counter – Operation of a PLC counter – Counter parameters [2 Hrs]

Format of counter instruction and counter data file [2 Hrs]

count up (CTU) – count down (CTD) simple Problems using counter. [2 Hrs]

UNIT IV

ADVANCED INSTRUCTION **[12 HRS]**

Introduction – Comparison instructions – Addressing format [2 Hrs]
for micro logic system

Different addressing types – Data movement instructions - [2 Hrs]
mathematical instructions

Program flow control instructions – PID instructions [1 Hr]

Program development and execution using Allen bradly PLC. [2 Hrs]

Simplified start up process of a coal feeding of a boiler plant [2 Hrs]

Elevator for 3 floor building – Traffic light control – Conveyor belt [2 Hrs]

Selection of PLC – Safety consideration built in the PLC's. [1 Hr]

UNIT V

I/O MODULE COMMUNICATION AND NETWORKING **[12 HRS]**

Introduction – Classification of I/O module input – output system [2 Hrs]

Direct I/O,Parallel I/O – Sourcing and sinking of serial I/O system.

PLC interfacing – Discrete input module – DC – AC – Discrete [2 Hrs]

output module - analog input module single ended and output module [2 Hrs]

RTD input module - Thermocouple – High speed encoder
Stepper motor – RS-232 interface module

Differential input module – Types of communication interface [1 Hr]

Parallel – Serial – IEEE 488 bus – serial balanced – unbalanced

Communication mode - Simplex – Half duplex [2 Hrs]

Full duplex features of good interface [1 Hr]

Serial interface RS232c. DB-9 connection of RS232

Network topology, Bus, ring, Star, Tree [2 Hrs]

Revision and Test **[12 Hrs]**

TEXT BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Introduction to Programmable Logic Controller	Gary Dunning	Thomson Delmar learning, Second Edition, 2008
2.	Programmable Logic Controller	FrankD.Petruzella	Tata MC Graw Hill, Third Edition, 2010

REFERENCE BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Programmable Logic Controllers; Principles and applications	Jhon W Webb Ronald A Rels	PHI Learning Pvt. Ltd. 2012
2.	Exploring Programmable Logic Controllers with Applications	Srivastava	BPB Publishers, 2012
3.	Programmable Logic Controller	Vijay R Yadhav	Khanna Publishers, 2010
4.	Programmable Logic Controllers	Gray Dunning	Tata MC Graw Hill, 2009

Learning website
https://unitronicsplc.com/what-is-plc-programmable-logic-controller/

https://www.elprocus.com/understanding-a-programming-logic-controller/

https://www.allaboutcircuits.com/textbook/digital/chpt-6/programmable-logic-controllers-plc/

https://www.engineersgarage.com/articles/plc-programmable-logic-controller

https://electrical-engineering-portal.com/download-center/books-and-guides/siemens-basics-of-energy/basics-of-plcs

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C542.1	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C542.2	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C542.3	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C542.4	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C542.5	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C542	**15**	**10**	**10**	**10**	**15**	**10**	**15**	**10**	**15**	**10**
Correlation Level	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECC 543 BIO MEDICAL INSTRUMENTATION

TEACHING AND SCHEME OFEXAMINATION:

Number of weeks per Semester: 15 weeks

Course	Instruction		Examination			
Bio Medical Instrumentation	Hrs/ week	Hrs/ semester	Marks			Duration
			Internal assessment	Semester end examination	Total	
	5	75	25	75	100	3Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME(Hrs)
I	Bio - electric signals, electrodes and clinical measurement	13
II	Bio - medical recorders	13
III	Therapeutic instruments	13
IV	Biotelemetry and patient safety	12
V	Modern imaging techniques	12
Revision and Test		12
Total		**75**

COURSE DESCRIPTION

Bio medical engineering education is in the growing stage. But every year, there is a tremendous increase in the use of modern medical equipment in the hospital and health care industry therefore it is necessary for every student to understand the functioning of various medical equipments. This subject to enable the students to learn the basic principles of different biomedical instruments viz Clinical measurement, Bio - medical recorders, Therapeutic instruments, Biotelemetry and Modern imaging techniques instruments.

OBJECTIVES

After learning this subject the student will be able to understand the about

- The generation of Bio-potential and its measurement using various electrodes.
- The measurement of blood pressure.
- The measurement of lung volume.
- The measurement of respiration rate.
- The measurement of body temperature and skin temperature.
- The principles of operations of ECG recorder.
- The principles of operations of EEG recorder.
- The principles of operations of ENG recorder.
- The working principles of audio meter.
- The principles of operations of pacemaker.
- The basic principle of dialysis.
- The basic principle of short wave diathermy.
- The basic principle of ventilators.
- The working principles of telemetry.
- The basic principle of telemedicine.
- To learn about patient safety.
- The various methods of accident prevention.
- The basic principle of various types of lasers.
- The basic principle of CT and MRI scanner.
- The principle of operation of various imaging techniques

COURSE OUTCOMES

ECC 543 BIO MEDICAL INSTRUMENTATION	
C 543.1	Explain the bio-electric signals and electrodes and clinical measurement
C 543.2	Interpret the Bio - medical recorders
C 543.3	Show the knowledge on Therapeutic instruments
C 543.4	Infer the concepts of biotelemetry and patient safety.
C 543.5	Explain about the Modern Imaging Techniques

ECC 543 BIO MEDICAL INSTRUMENTATION

UNIT-I

BIO-ELECTRIC SIGNALS AND ELECTRODES **[13 Hrs]**

Elementary ideas of cell structure, Bio – potential and their generation [2 Hrs]

resting and action potential – propagation of action potential. [2 Hrs]

Electrodes – Micro – Skin surface – needle electrodes. [2 Hrs]

CLINICAL MEASUREMENT:

Measurement of Blood pressure (direct, indirect) [2 Hrs]

blood flow meter (Electro magnetic& ultrasonic blood flow meter)

blood pH measurement - Measurement of Respiration rate [2 Hrs]

measurement of lung volume – heart rate measurement

Measurement of body and skin temperature – [2 Hrs]

Chromatography, Photometry, Flurometry. [1 Hr]

UNIT-II **[13 Hrs]**

BIO - MEDICAL RECORDERS:

Electro cardiograph (ECG) – Lead system – ECG electrodes – [2 Hrs]

ECG amplifiers – ECG recording units – analysis of ECG curves. [2 Hrs]

Nervous system – EEG recorder – 10-20 lead system – recording techniques – [2 Hrs]

EEG wave types – Clinical use of EEG – brain tumour Electro – [2 Hrs]

myograph (EMG) – EMG waves – measurement of conduction velocity – [1 Hrs]

EMG recording techniques – [2 Hrs]

Electro – retinograph (ERG) Audiometer – principle – types –

Basics audiometer working. [2 Hrs]

UNIT-III

THERAPEUTIC INSTRUMENTS: **[13 Hrs]**

Cardiac pacemaker – classification – External pace makers – [2 Hrs]

implantable pacemaker – pacing techniques – programmable pacemaker [2 Hrs]

Cardiac defibrillators – types – AC and DC defibrillators – [2 Hrs]

Heart lung machine with Block diagram. Dialysis – [2 Hrs]

Hemo dialysis – peritoneal dialysis.

Endoscopes Endoscopic laser coagulator and applications [2 Hrs]

physiotherapy equipment – short wave diathermy

micro wave diathermy – ultrasonic therapy unit (block / circuit) [2 Hrs]

Ventilators – types – modern ventilator block diagram. [1 Hr]

UNIT-IV

BIOTELEMETRY AND PATIENT SAFETY **[12 Hrs]**

Introduction to biotelemetry – physiological – adaptable to biotelemetry [2 Hrs]

components of a biotelemetry system – application of telemetry

elements of biotelemetry; AM, FM transmitter and receiver

requirements for biotelemetry system – radio telemetry with sub carrier [2 Hrs]

single channel and multi channel telemetry

Telemedicine; introduction, working, applications.

Patient safety: Physiological effects of electric current – Micro and macro shock [2 Hrs]

leakage current – shock hazards from electrical equipment.

Methods of Accident Prevention – Grounding – Double Insulation [2 Hrs]

Protection by low voltage – Ground fault circuit interrupter

Isolation of patient connected parts – Isolated power distribution system. [2 Hrs]

Safety aspects in electro surgical units [1 Hr]

burns, high frequency current hazards, Explosion hazards. [1 Hr]

UNIT-V **[12 Hrs]**

MODERN IMAGING TECHNIQUES:

LASER beam properties – block diagram – operation of CO2 and NDYag LASER [2 Hrs]

applications of LASER in medicine. X ray apparatus – block diagram – operation [3 Hrs]

special techniques in X-ray imaging – Tomogram – computerized Axial tomography [3 Hrs]

Ultrasonic imaging techniques – Echo cardiography – Angiography [2 Hrs]

CT scanner - Magnetic resonance imaging techniques. [2 Hrs]

Revision and Test **[12 Hrs]**

TEXT BOOKS:

Si.No	Title	Author	Publisher with Edition
1.	Biomedical Instrumentation	Dr.M. Arumugam	Anuradha publications, chennai edition, 2003

REFERENCE BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Biomedical Instrumentation and measurement	Leslie Cromwell – Fred.J. Weibell, ErichA.P Feither	IIedition,Pearson education,2008
2.	Medicine and clinical Engineering	Jacobson and Webstar	PHI publishers, 2010
3.	Hand book of Bio – Medical Instrumentation .	R.S .Khandpur	CBS publications, 1st edition ,2007
4.	Medical Electronics	Kumara doss	Tata mcgraw hill, 2nd edition, 2003
5.	Introduction to Medical Electronics	B.R. Klin	IV edition, pearson education, 2008
6.	Introduction to Biomedical Instrumentation	Mandeep Singh	Printice Hall India 2010.

LEARNING WEBSITE

1. https://collegegrad.com/careers/biomedical-engineers
2. https://www.careers360.com/biomedical-engineering-course
3. https://www.mtu.edu/biomedical/department/what-is/ https://collegedunia.com/courses/bachelor-of-engineering-be-biomedical-engineering
4. https://www.sarvgyan.com/courses/engineering/biomedical-engineering

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**
			---.

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 543.1	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C 543.2	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C 543.3	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C 543.4	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C 543.5	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**
C 543	**15**	**10**	**10**	**10**	**15**	**10**	**15**	**10**	**15**	**10**
Correlation Level	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**2**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 550 ADVANCED COMMUNICATION SYSTEMS PRACTICAL

TEACHING AND SCHEME OFEXAMINATION:

Number of Weeks/ Semester : 15 Weeks

Course	Instruction		Examination			
			Marks			Duration
	Hours/ Weeks	Hours/ Semester	Internal Assessment	End semester Examination	Total	
Advanced Communication Systems Practical	4	60	25	75	100	3Hrs

ALLOCATION OF MARKS

CIRCUIT DIAGRAM/BLOCK DIAGRAM :	20
CONNECTION:	25
EXECUTION & HANDLING OF EQUIPMENT:	15
OUTPUT / RESULT:	10
VIVA – VOCE:	05
TOTAL	**75**

COURSE DESCRIPTION:

Today advanced communication systems has developed to a great extent that there is always need to construct various communication concepts. This subject fulfils the need for students to have a thorough knowledge of ASK, FSK,PSK,TDM,PCM,PWM. In addition, the course will provide the students with necessary knowledge and installation of DTH system and construct LED characteristics.

MAJOR EQUIPMENTS REQUIRED

S.No	Name of the Equipments	Range	Required Nos
1.	Regulated power supply	(0-30v)	05
2.	Dual Trace CRO	-	02
3.	Signal Generator	1MHZ	01
4.	Fiber optics Kit	-	01
5.	PCM Trainer Kit	-	01
6.	ASK modulation & Demodulation kit	-	01
7.	FSK Modulation & Demodulation kit	-	01
8.	PSK Modulation & Demodulation kit	-	01
9.	Manchester encoder and decoder	-	01
10.	DTH system		01

OBJECTIVES

- To construct the ASK, FSK & PSK
- To construct Sample and Hold Circuit.
- To construct various digital modulation techniques.
- To measure the losses and numerical aperture of optical fiber
- To learn the LED and Photodiode characteristics .
- To construct .a voice link using optical fiber
- Configure a analog and digital link setup
- Install the process of DTH system

COURSE OUTCOMES

ECC 550 ADVANCED COMMUNICATION SYSTEMS PRACTICAL

After successful completion of this course, the students should be able to

C 550.1 Construct ASK,FSK,PSK Modulation/Demodulation circuits and analyze output waveforms.

C 550.2 Construct TDM ,PCM,PWM ,LED circuits and determine output.

C 550.3 Construct fiber optic analog link and fiber optic digital link, bending loss, propagation loss, Numerical aperture, Manchester encoder and decoder.

C 550.4 Construct and test analog transmitter ,receiver and test a voice link using fibre.

C 550.5 Demonstrate the installation DTH system .

ECC 550 ADVANCED COMMUNICATION SYSTEMS PRACTICAL

List of Experiments :

S.No	Name of the experiment	Course Outcome
1.	Trace the output waveform of ASK modulation & demodulation circuit.	C550.1
2.	Trace the output waveform of FSK modulation circuit.	C550.1
3.	Trace the output waveform of FSK demodulation circuit.	C550.1
4.	Trace the output waveform of PSK modulation circuit.	C550.1
5.	Trace the output waveform of PSK demodulation circuit.	C550.1
6.	Construct the circuit to determine the output of a TDM signal.	C550.2
7.	Trace the output waveform of PCM Signal.	C550.2
8.	Trace the output of a Pulse width modulated Signal.	C550.2
9.	Construct and test a fiber optic analog link.	C550.3
10.	Construct and test a fiber optic digital link.	C550.3
11.	Construct and test analog transmitter and receiver.	C550.4
12.	Construct a suitable circuit & find the bending loss and propagation loss in fiber optics.	C550.3
13.	Construct and measure the Numerical aperture of optical fiber.	C550.3
14.	Construct and test the performance of Manchester encoder and decoder.	C550.3
15.	Construct and test a voice link (with telephone handset both at transmitter and receiver using optical fiber)	C550.4
16.	Install a DTH system. & test it.	C550.5
17.	Construct a LED circuit to find the photo diode characteristics.	C550.2

LEARNING WEBSITES

1.https://ajaybolar.weebly.com/uploads/1/0/1/0/10106930/advanced_communication_lab_manual-10ecl67..pdf

2.https://lecturenotes.in/subject/74/advanced-communication-system-acs/practical

3.https://www.abebooks.com/first-edition/Advanced-Communication-Lab-Manual-Preeta-Sharan/8137584768/bd

4.http://www.sbtebihar.gov.in/Syllabus/6th-Sem/6S-38-Electronics-&-Communication-Engineering.pdf

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

m) Attendance : 5 marks – (Award of marks same as theory subjects)

n) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

o) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 550.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C 550.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C 550.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C 550.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C 550.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C 550	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**10**	**15**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECC 560 MICROCONTROLLER PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

Number of Weeks/ Semester : 15 Weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Micro Controller Practical	4	60	25	75	100	3 Hrs

ALLOCATION OF MARKS

ALGORITHM OR FLOW CHART :	15 MARKS
PROGRAM	25 MARKS
EXECUTION	20 MARKS
RESULT	10 MARKS
VIVA	5 MARKS
TOTAL	75 MARKS

COURSE DESCRIPTION:

Today Microcontroller Engineering has developed to a great extent that there is always the need for study of various controller concepts. This lab is fulfill the need for students to write the assembly language programme for Multibyte Addition, Multiplication, Division, BCD to HEX,ASCII to Binary and execute the same in 8051 kit and also write the assembly language programme for Interfacing Digital I/O board, ADC, DAC, Stepper Motor etc.,

MAJOR EQUIPMENTS REQUIRED

S.No	Name of the Equipments	Range	Required Nos
1.	8051 Microcontroller Kit	-	14 Nos
2.	Digital I/O Interface Board	-	02 Nos
3.	Matrix keyboard Interface Board	-	02 Nos
4.	Seven segment LED display Interface Board	-	02 Nos
5.	Traffic light Interface Board	-	02 Nos
6.	8 bit ADC Interface Board	-	02 Nos
7.	8 bit DAC Interface Board	-	02 Nos
8.	Stepper Motor Control Interface Board	-	02 Nos
9.	DC motor control Interface Board	-	02 Nos
10.	RS232 serial port cable	-	02 Nos

Objectives

- Write the assembly language programme for Multibyte addition, Multiplication, Division, Ascending order.
- Write the assembly language programme for the conversions like BCD to HEX,HEX to BCD,ASCII to Binary.
- Write the assembly language programme for Parity generation & Timer, Counter and also the above programmes are executed by using 8051 microcontroller kit.
- Write the assembly language programme for Interfacing Digital I/O Board, Matrix Keyboard, Seven Segment LED Display ,Traffic Light control, ADC, DAC, Stepper Motor, DC Motor and test it with Application Boards.

COURSE OUTCOME

ECC 560 MICROCONTROLLER PRACTICAL

After successful completion of this course, the students should be able to

C 560.1	Develop an Assembly Language Program and execute in 8051.(additionsubtraction,multiplication,division,ascending order)
C 560.2	Develop an Assembly Language Program and execute in 8051.(ASCII to Binary, BCD to Hexadecimal,parity bit generation)
C 560.3	Develop an Assembly Language Program for timer/counter and execute in 8051
C 560.4	Develop an Assembly Language Program for interfacing.(Digital I/O board, Matrix keyboard, seven segment LED, Traffic light control, 8 bit ADC/DAC)
C 560.5	Develop an Assembly Language Program for interfacing.(Stepper motor, DC motor, IR sensor, Sending data through serial port

ECC 560 MICRO CONTROLLER PRACTICAL

Part-A

S.No	Name of the experiment	Course Outcome
1.	Write an Assembly Language Program for Multi-byte Addition and execute the same in the 8051 Kit.	C560.1
2.	Write an Assembly Language Program for Multiplication and Division of two numbers and execute the same in the 8051 Kit.	C560.1
3.	Write an Assembly Language Program for Arranging the given data in Ascending order and execute the same in the 8051 Kit.	C560.1
4.	Write an Assembly Language Program for ASCII to Binary and execute the same in the 8051 Kit.	C560.2
5.	Write an Assembly Language Program for BCD to Hexadecimal and execute the same in the 8051 Kit.	C560.2
6.	Write an Assembly Language Program for Parity bit generation and execute the same in the 8051 Kit.	C560.2
7.	Write an Assembly Language Program for using timer / Counter and execute the same in the 8051 Kit.	C560.3

Part – B

INTERFACING WITH APPLICATION BOARDS

S.No	Name of the experiment	Course Outcome
8.	Write an Assembly Language Program for interfacing Digital I/O board and test it.	C560.4
9.	Write an Assembly Language Program for interfacing Matrix keyboard and test it.	C560.4
10.	Write an Assembly Language Program for interfacing seven segment LED displays and test it.	C560.4
11.	Write an Assembly Language Program for interfacing Traffic light control and test it.	C560.4
12.	Write an Assembly Language Program for interfacing 8 bit ADC and test it.	C560.4
13.	Write an Assembly Language Program for interfacing 8 bit DAC and test it.	C560.4
14.	Write an Assembly Language Program for interfacing Stepper motor and test it.	C560.5
15.	Write an Assembly Language Program for interfacing DC motor and test it.	C560.5`
16.	Write an Assembly Language Program for Sending data through serial port between controller kit and test it	C560.5
17.	An application oriented project for interfacing an IR sensor with 8051.	C560.5

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

g) Attendance : 5 marks – (Award of marks same as theory subjects)

h) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

i) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 560.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C 560.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C 560.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C 560.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C 560.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**
C 560.1	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**10**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

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ECC 570 VERY LARGE SCALE INTEGRATION PRACTICAL

TEACHING AND SCHEME OFEXAMINATION:

Number of Weeks/ Semester : 15 Weeks

Course	Instruction		Examination			
	Hours/ Weeks	Hours/ Semester	Marks			Duration
			Internal Assessment	End semester Examination	Total	
Very Large Scale Integration Practical	4	60	25	75	100	3Hrs

ALLOCATION OF MARKS

INTERFACE CIRCUIT DIAGRAM	10 MARKS
ALGORITHM OR FLOW CHART	20 MARKS
PROGRAM	20 MARKS
EXECUTION	10 MARKS
RESULT	10 MARKS
VIVA VOCE	5 MARKS
TOTAL	**75** MARKS

Course Description:

VHDL is a versatile and powerful hardware description language which is useful for modeling digital systems at various levels of design abstraction. This language is for describing the structural, simulation of the digital system allows us to validate the design prior to fabrication of Digital Integrated circuit. This practical introduces basic on VHDL concepts and constructs. It introduces the VHDL from simulation cycle to synthesis level in combinational and sequential circuits.

MAJOR EQUIPMENTS REQUIRED

S.No	Name of the Equipments	Range	Required Nos
1.	FPGA KIT with atleast 10 switches for input, 8 LEDs for output, a 7 segment display, debounced push switch (2 Nos) for manual clock input and external clock source.	-	10 Nos.

OBJECTIVES

On successful completion of the course the students must be able to

- Simulation of VHDL code a combinational circuit
- Simulation of VHDL code a for Arithmetic Circuits
- Simulation of VHDL code a for Multiplexer.
- Implementation of Multiplexer /Demultiplexer
- Implementation of Decoder/ Encoder
- Implementation of half adder and half subtractor
- Implementation of full adder and full subtractor**.**
- Implementation of 7 segment decoder/7 segment decoder(LUT)
- VHDL Implementation of Blinking LED/ array OF LEDS
- VHDL implementation of 7 segment display/ delay

ECC 570 VERY LARGE SCALE INTEGRATION PRACTICAL

After successful completion of this course, the students should be able to

C 570.1 Build the VHDL code: Combinational Circuit, Arithmetic Circuits, Multiplexer/ Demultiplexer, Half adder and Half subtractor, Full Adder And Full Subtractor.

C 570.2 Design and implement VHDL Multiplexer/ Demultiplexer

C 570.3 Design and implement VHDL code for 7 segment decoder/7 segment decoder by LUT and Encoder

C 570.4 Design and implement VHDL code for delay, blinking a LED and testing a gate

C 570.5 Design and implement VHDL code for Delay & 7 segment display , Speller with array of LEDS, Blinking array of LEDS.

ECC 570 VERY LARGE SCALE INTEGRATION PRACTICAL

1. **SIMULATION OF VHDL CODE FOR COMBINATIONAL CIRCUIT** **Course Outcome** C 570.1

   Optimize a 4 variable combinational function (SOP or POS), describe it in VHDL code and simulate it. Example: F= (0,5,8,9,12) in sop or pos

2. **SIMULATION OF VHDL CODE FOR ARITHMETIC CIRCUITS** C 570.1

   Design and Develop the circuit for the following arithmetic function in VHDL Codes and Simulate it. Addition, Subtraction Multiplication (4 x 4 bits)

3. **SIMULATION OF VHDL CODE FOR MULTIPLEXER** C 570.1

   Design and develop a 2 bit multiplexer and portmap the same for developing upto 8 bit multiplexer.

4. **SIMULATION OF VHDL CODE FOR DEMULTIPLEXER** C 570.1

   Design and develop an 8 output demultiplexer. Simulate the same code in the software

5. **SIMULATION OF VHDL CODE FOR HALF ADDER AND HALF SUBTRACTOR.** C 570.1

   Design and develop half adder and half subtractor and Simulate the same code in the software

6. **SIMULATION OF VHDL CODE FOR FULL ADDER AND FULL SUBTRACTOR.** C 570.1

   Design and develop full adder and full subtractor and Simulate the same code in the software

7. **VHDL IMPLEMENTATION OF MULTIPLEXER** C 570.2

   Describe the code for a multiplexer and implement it in FPGA kit in which switches are connected for select input and for data inputs a LED is connected to the output.

8. **VHDL IMPLEMENTATION OF DEMULTIPLEXER** C 570.2

   Switches are connected for select inputs and a data input, Eight LEDs are connected to the output of the circuit.

9. **VHDL IMPLEMENTATION OF 7 SEGMENT DECODER** C 570.3

   Develop Boolean expression for 4 input variables and 7 output variables. Design and develop a seven segment decoder in VHDL for 7 equations. A seven segment display is connected to the output of the circuit. Four switches are connected to the input. The 4 bit input is decoded to 7 segment equivalent.

10. VHDL IMPLEMENTATION OF 7 SEGMENT DECODER BY LUT C 570.3

Develop a 7 segment decoder using Look up table. Describe the seven segment decoder in VHDL using developed Look up table. A seven segment display is connected to the output of the circuit. Four switches are connected to the input. The 4 bit input is decoded into 7 segment equivalent.

11. VHDL IMPLEMENTATION OF ENCODER C 570.3

Design and develop HDL code for decimal (Octal) to BCD encoder. There will be10 input switches (or 8 switches) and 4 LEDs in the FPGA kit. The input given from switches and it is noted that any one of the switch is active. The binary equivalent for the corresponding input switch will be glowing in the LED as output.

12. SIMULATION OF VHDL CODE FOR DELAY C570.4

Develop a VHDL code for making a delayed output for 1second or 2 seconds by assuming clock frequency provided in the FPGA Kit.

13. VHDL IMPLEMENTATION FOR BLINKING A LED C570.4

Develop a VHDL Code for delay and verify by simulating it. This delay output is connected to LED. Delay is adjusted such away LED blinks for every 1 or 2 seconds.

14. SIMULATE A VHDL TEST BENCH CODE FOR TESTING A GATE C570.4

Develop a VHDL test bench code for testing any one of the simple gate. Simulate the test bench code in the HDL software.

15. VHDL IMPLEMENTATION FOR BLINKING A ARRAY OF LEDS C570.5

Design and develop a VHDL Code for 4 bit binary up counter. Four LEDs are connected at the output of the counter. The counter should up for every one seconds.

16. VHDL IMPLEMENTATION OF A SPELLER WITH AN ARRAY OF LEDS C570.5

Design and develop VHDL Code for a 5 bit Johnson ring counter 4 bit The LEDs are connected at the output of the counter. The speller should work for every one seconds.

17. VHDL IMPLEMENTATION OF 7 SEGMENT DISPLAY C570.5

Design and develop a seven segment decoder in VHDL. Design and develop a 4 bit BCD counter, the output of the counter is given to seven segment decoder. A seven segment display is connected to the output of the decoder. The display shows 0,1, 2.. 9 for every one second

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

a) Attendance : 5 marks – (Award of marks same as theory subjects)

b) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

c) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C570.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C570.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C570.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C570.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C570.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**
C570 Total	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**10**	**15**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

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ECC 510 ADVANCED COMMUNICATION SYSTEMS
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
17.	What is RADAR ?	I	U
18.	What is ISDN?	I	U
19.	Give example for optical source	III	R`
20.	Define apogee.	IV	R
21.	What is roaming?	V	U
22.	What is TDMA?	V	U
23.	What is GSM?	V	U
24.	Name different types of orbit.	IV	R

PART-B (5x3=15Marks)
Answer any 5 Questions

S.No		Unit	Bloom's Level
25.	What is duplexer?	I	U
26.	Write down the equation for channel capacity.	I	R
27.	What is graded index fiber?	II	U
28.	What are the uses of facsimile communication system?	III	U
29.	What is fiber splice?	IV	U
30.	Compare surface emitter and edge emitter LEDs.	IV	An
31.	Mention the disadvantages of passive satellite.	V	U
32.	Explain the term hand off.	V	U

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	With the Block Diagram Explain Pulsed Radar System.	I	U	10
		(OR)			
	B.	Explain Electronics Switching System With the Block Diagram.	I	U	10
18	**A.**	Draw the Block Diagram Of FSK Modulation And Explain Each Block.	II	U	10
		(OR)			
	B.	Explain Forward Error Correcting Code and Hamming Code	II	U	10
19.	**A.**	Explain the Block Diagram of Optical Transmitter and Receiver.	III	U	10
		(OR)			
	B.	Explain the Principle of light transmission in fiber using ray theory	III	U	10
20.	**A.**	Briefly Explain Kepler's I, II and III Laws.	IV	R	10
		(OR)			
	B.	With the Block Diagram Explain Transmit –Receive Earth Station.	IV	U	10
21.	**A.**	Explain the fundamental concepts of cellular telephone system.	V	U	10
		(OR)			
	B.	Draw the architecture of GSM system and explain its operation.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 520 MICROCONTROLLER
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
1.	What is microcontroller?	I	U
2.	What are the addressing modes of 8051?	I	R
3.	What is assembler?	III	U`
4.	What are the modes of programming of timer?	III	R
5.	Mention Counter programming.	III	U
6.	State the use of interrupts in 8051.	IV	R
7.	What is RS 232C?	IV	U
8.	What are the modes of 8255?	II	U

PART-B (5x3=15Marks)
Answer any 5 Questions

S.No		Unit	Bloom's Level
9.	Explain about program counter ?	I	U
10.	Write program about the 8 bit Multiplication of 2 nos?	I	U
11.	Explain ASCII to BINARY Conversion.	II	U
12.	How can you perform Mode 2 Programming?	III	R
13.	Mention the SFR registers used in timer operation?	IV	U
14.	What is the function of C/T bit in TMOD register?	IV	AP
15.	Draw the RS232 connection to 8051?	V	U
16.	Explain the Dc Motor interfacing using PWM?	V	U

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	Explain the Block diagram of 8051 Microcontroller.	I	U	10
		(OR)			
	B.	Explain the Classification of 8051 instructions.	I	U	10
18	**A.**	Explain the different addressing modes of 8051.	II	U	10
		(OR)			
	B.	Explain Multibyte addition with program	II	U	10
19.	**A.**	Explain Bit addresses for I/O & RAM.	III	U	10
		(OR)			
	B.	Explain the programming of Timer.	III	U	10
20.	**A.**	Explain about 8051 Serial communication Programming.	IV	U	10
		(OR)			
	B.	Explain Interrupt priority in 8051.	IV	U	10
21.	**A.**	Explain IC 8255 with Block diagram.	V	U	10
		(OR)			
	B.	Explain about the Stepper motor interfacing with 8051.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 530 VERY LARGE SCALE INTEGRATION
MODEL OUESTION PAPER

Time : 3 Hrs **Max marks : 75**

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
1.	What are universal gates?	I	U
2.	Define encoder.	I	R
3.	Expand VHDL.	II	R
4.	Draw the circuit for half adder.	I	R
5.	Define state table.	III	U
6.	Define serial adder.	IV	U
7.	Define PLA.	V	U
8.	Expand ASIC.	V	U

PART-B (5x3=15Marks)
Answer any 5 Questions

S.No		Unit	Bloom's Level
9.	What do you mean by hazards in digital circuit?	I	U
10.	Define multiplexer.	I	U
11.	Distinguish between combinational circuits and sequential circuits.	III	AP
12.	Define Timing simulation.	II	R
13.	What do you mean by SISO & PISO?	IV	U
14.	Write the excitation table for D Flipflop?	III	U
15.	Define Moore type FSM.	III	U
16.	Give two examples for custom chip.	III	U

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	Implement the function f = ∑(1, 2, 3,5, 7,10,13) with do not care 4 & 6 with minimal gates.	I	AP	10
		(OR)			
	B.	Draw the circuit of NMOS NAND, NOR,AND & OR.	I	U	10
18	**A.**	Explain in detail about assignment statements.	II	U	10
		(OR)			
	B.	i)Write a VHDL code four bit comparator.	II	AP	10
		ii) Write a VHDL code four bit adder.		AP	
19.	**A.**	Design a modulo 8 bit counter using D flip flop. Use proper excitation table & state diagram.	III	C	10
		(OR)			
	B.	Explain about the moore & mealy machine and give out the examples.	III	U	10
20.	**A.**	Write down the VHDL code for modulo 6 bit up/down counter.	IV	U	10
		(OR)			
	B.	Write down the VHDL code for serial adder.	IV	AP	10
21.	**A.**	Implement the function F= ∑ m (0,1,2,3,5) in PAL.	V	An	10
		(OR)			
	B.	Explain about CPLD and FPGA in detail.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

ECC 541 DIGITAL COMMUNICATION
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
1.	What is digital communication?	I	U
2.	What is an echo compressor?	I	R
3.	Define sampling?	III	U`
4.	What is burst error?	III	R
5.	What is PCM?	III	U
6.	What is E1 framing?	IV	R
7.	What is MSK?	IV	U
8.	What is spread spectrum communication?	II	U

PART-B (5x3=15Marks)
Answer any 5 Questions

S.No		Unit	Bloom's Level
9.	What are the functions performed during the process of ADC?	I	U
10.	What is meant by aliasing?	I	U
11.	Explain the forward error correction.	II	U
12.	Explain the m-ary pulse modulation.	III	R
13.	What is meant by CRC?	IV	U
14.	What are the modulation techniques used in digital communication?	IV	U
15.	Explain balance property and correlation property.	V	U
16.	Write about jamming consideration	V	U

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	Draw and explain the block diagram of digital communication system.	I	U	10
		(OR)			
	B.	Explain briefly about synchronous and asynchronous communication.	I	U	10
18	**A.**	Explain the Delta modulation transmitter and receiver with block diagram.	II	U	10
		(OR)			
	B.	Explain DM receiver and transmitter with block diagram and state DM advantages and disadvantages.	II	U	10
19.	**A.**	Explain MSK transmitter and receiver with block diagram.	III	AP	10
		(OR)			
	B.	Draw and explain the block diagram of QPSK transmitter	III	U	10
20.	**A.**	Explain Retransmission and Forward error correcting code.	IV	U	10
		(OR)			
	B.	Explain baudot code and mention its drawbacks and limitations.	IV	U	10
21.	**A.**	Explain OSI model or Layered Architecture.	V	U	10
		(OR)			
	B.	Write notes circuit Switching and store and forward switching.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 542 PROGRAMMABLE LOGIC CONTROLLERS
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
1.	State the use of PLC.	I	U
2.	Expand DAS .	I	R
3.	Expand SCADA.	III	U`
4.	Draw the symbol of Float switch	III	R
5.	Mention some transmission media.	III	U
6.	What is meant by PLC counter?	IV	R
7.	What is the classification of network?	IV	AP
8.	Write any two advantage of SCADA.	II	U

PART-B (5x3=15Marks)
Answer any 5 Questions

S.No		Unit	Bloom's Level
9.	What is the function of analog input module?	I	U
10.	List the different types of programming methods of PLC	I	U
11.	Draw the symbol for PLC comparator	II	U
12.	What is communication protocol?	III	R
13.	Write about Direct Digital Controller	IV	U
14.	Mention the output address scheme of Siemens Micro PLC	IV	U
15.	Which field bus is required with distributed control system?	V	U
16.	List the various types of PLC.	V	U

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	Discuss in detail about advantages of PLC over hardwired system.	I	U	10
		(OR)			
	B.	Draw the basic block diagram of PLC and give brief account on each block.	I	U	10
18	**A.**	Draw the discrete input module and explain the operation.	II	U	10
		(OR)			
	B.	Discuss in detail about various output module of PLC.	II	U	10
19.	**A.**	Explain ON delay and OFF delay timer instructions with simple examples.	III	AP	10
		(OR)			
	B.	Explain briefly about the operation of PLC counter.	III	U	10
20.	**A.**	Describe about the addressing format for micro logic system.	IV	U	10
		(OR)			
	B.	Explain about the Selection of PLC and Safety consideration built in the PLC's	IV	U	10
21.	**A.**	Explain about the Network topology of Bus, ring, Star, Tree.	V	U	10
		(OR)			
	B.	Discuss in detail about PLC interfacing.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs) R-Remember, U-Understand , Ap-Apply	Higher Order Thinking Skills (HOTs) An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 543 BIOMEDICAL INSTRUMENTATION
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)

Answer any 5 Questions

S.No		Unit	Bloom's Level
1.	What are electrodes ?	I	U
2.	What is Chromotogtraphy?	I	R
3.	What is the Principle of ERG?	III	U`
4.	What are the types of defibrillators?	III	R
5.	What is Short wave diathermy?	III	U
6.	Define Radiotelemetry?	IV	R
7.	What are the methods of accident prevention?	IV	U
8.	Define Echo cardigraphy ?	II	U

PART-B (5x3=15Marks)
Answer any 5 Questions

S.No		Unit	Bloom's Level
9.	Explain about Biopotential and its generation?	I	U
10.	Explain about photometery?	I	U
11.	Explain EEG recorder?	II	U
12.	What are External pacemakers?	III	R
13.	Mention the types of ventilators?	IV	U
14.	What is the function of biotelemetry?	IV	U
15.	What are thesafety measures for explosion hazards?	V	U
16.	Explain the CT scanner?	V	U

PART-C (5x10=50 Marks)

Answer all Questions choosing either division (A) or division (B) of each question

S. No			Unit	Bloom's Level	Max marks
17.	**A.**	Explain about action & resting potential?	I	U	10
		(OR)			
	B.	Explain with diagram of blood PH measurement?	I	U	10
18	**A.**	Explain the ECG with neat diagram.	II	U	10
		(OR)			
	B.	Explain about ERG & audiometer	II	U	10
19.	**A.**	Explain about Cardiac Pacemaker	III	U	10
		(OR)			
	B.	Explain the working of Ultrsonic theorapy	III	U	10
20.	**A.**	Explain about the elements of biotelemetrysystem.	IV	U	10
		(OR)			
	B.	Explain about the Isolated power distribution system	IV	U	10
21.	**A.**	Explain the block diagram of LASER.	V	U	10
		(OR)			
	B.	Explain about the Magnetic resonance imaging techniques	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy Level	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECC 610 EMBEDDED SYSTEMS

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 Weeks

Course	Instruction		Examination			
	Hrs/ Weeks	Hrs/ Semester	Marks			Duration
			Internal Assessment	Semester End Examination	Total	
Embedded Systems	6	90	25	75	100	3Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME(Hrs)
I	ARM processor Architecture	16
II	ARM instruction set and interrupts	16
III	Catch mechanism and Memory Protection and Management unit	16
IV	LPC 2148 ARM processor	16
V	Embedded OS and RTOS	14
Revision Test		12
Total		**90**

Course Description:

Increasingly, embedded systems developers and system-on-chip designers select specific microprocessor cores and a family of tools, libraries, and off-the-shelf components to quickly develop embedded system-based products. A major processor in this industry is ARM. Since 1985, the ARM architecture has become the most pervasive 32-bit architecture in the world. ARM processors are embedded in products ranging from cell/mobile phones to automotive Braking systems. A worldwide community of ARM partners and third-party vendors has Developed among semiconductor and product design companies, including hardware engineers, System designers, and software developers. This course has been to describe the operation of the ARM core from a product developer's perspective with a clear emphasis on its architecture by assuming no previous ARM experience.

OBJECTIVES:

- On successful completion of the course, the students must be able to
- Distinguish between CISC and RISC architecture
- Understand the ARM design philosophy
- Explain the ARM architecture and the pipeline structure
- Describe the little and big endian methods of representation
- Explain the Instruction sets of ARM processor.

- Understand various operational modes in ARM processor
- List the various exceptions and handling methods
- Develop an assembly level code for basic arithmetic primitive operations
- Understand the cache mechanism and cache policies
- List and explain various cache mechanisms
- Explain the essential of cache memory, write buffers and its policie
- Explain the importance of Lockdown and its method.
- Explain the importance of MPU and MMU
- Understand the functionality of virtual memory.
- Relate and distinguish between OS and RTOS in their functionality.
- Understand hard time and soft time RTOS.
- Explain multitasking, scheduling, ITC, and synchronization.
- Develop simple application in RTOS.

COURSE OUTCOMES

ECC 610 EMBEDDED SYSTEMS	
After successful completion of this course, the students should be able to	
C 610.1	Explain ARM processor architecture and fundamentals.
C 610.2	Interpret ARM instructions sets, interrupts, ARM processor exceptions and modes and develop simple programs..
C 610.3	Explain about cache mechanism and memory protection and management unit.
C 610.4	Explain about LPC 2148 ARM CPU and system control block functions.
C 610.5	Compare the concepts of embedded OS and RTOS.

ECC 610 EMBEDDED SYSTEMS

UNIT I

ARM PROCESSOR ARCHITECTURE **[16 Hrs]**

Concept of Embedded system design- design challenges [2 Hrs]

The RISC,CISC and ARM design

Philosophy, Embedded System Hardware -ARM Development tools [2 Hrs]

ARM PROCESSOR FUNDAMENTALS:

Data Flow model, Registers,modes of operation [2 Hrs]

Current Program Status Register, Pipeline [3 Hrs]

Exceptions, Interrupts, and the Vector Table [2 Hrs]

ARM nomenclature and families. Big Endian and Little Endian [3 Hrs]

ARM development tools [2 Hrs]

UNIT II

ARM INSTRUCTIONS SETS AND INTERRUPTS **[16 Hrs]**

ARM and Thumb Instruction Sets, Data Processing Instructions, [2 Hrs]

Branch Instructions, Load-Store Instructions [2 Hrs]

Software Interrupt Instruction, Program Status Register [2 Hrs]

Instructions, Conditional Execution, Stack Instructions [2 Hrs]

ARM PROCESSOR EXCEPTIONS AND MODES:

Vector table, Priorities, link Register offsets [3 Hrs]

Interrupts, and IRQ / FIQ exceptions interrupt [2 Hrs]

Stack design and implementation.

SIMPLE PROGRAM: Addition, Subtraction, Multiplication [2 Hrs]

UNIT III

CACHE MECHANISM AND MEMORY PROTECTION **[16 Hrs]**

AND MANAGEMENT UNIT

Introduction to cache memory, memory hierarchy and [2 Hrs]

Cache memory, Cache architecture and cache policies

CONCEPT OF FLUSHING AND CLEANING CACHE:

Flushing and Cleaning ARM cache core [1 Hr]

CONCEPT OF CACHE LOCKDOWN:

Locking Code and Data in Cache - Cache and write buffer [2 Hrs]

Stack and stack pointer

Comparison of cache and stack [1 Hr]

MEMORY PROTECTION AND MANAGEMENT UNIT

Introduction to Protection unit, Protected Regions, [1 Hr]

Demonstration of an MPU system [2 Hrs]

Components of MPU - Importance of MPU

Memory management unit block diagram [2 Hrs]

Main components of MMU – Definition of Virtual Memory [2 Hrs]

Virtual Memory - working principle [2 Hrs]

Memory size & speed - Importance of MMU [1 Hr]

UNIT IV

LPC 2148 ARM CPU **[16 Hrs]**

INTRODUCTION

Architectural overview [2 Hrs]

Memory mappig-block diagram [2 Hrs]

SYSTEM CONTROL BLOCK FUNCTIONS

PLL - Power control – Reset – VPB divider – Wakeup Timer [2 Hrs]

Memory Acceleration module – Timer 0 and Timer 1 – PWM [2 Hrs]

RTC – On chip ADC – On chip ADC – On chip DAC – Interrupts [2 Hrs]

Controller – General Purpose Input/Output(GPIO) [2 Hrs]

Universal Asynchronous Receiver/Transmitter [2 Hrs]

I^2C Interface [2 Hrs]

UNIT V

EMBEDDED OS AND RTOS **[14 Hrs]**

Fundamentals components to Embedded OS, [3 Hrs]

Simple Little Operating System: Initialization,

Memory model, interrupts and exceptions handling,

Scheduler, and context switch, performance issues

INTRODUCTION TO RTOS:

Real-time systems concepts, foreground/background systems, [3 Hrs]

Critical sections, resources, multitasking,

Context switching, scheduling, re-entrancy, [2 Hrs] Task priorities, mut

exclusion [2 Hrs]

SYNCHRONIZATION AND IPC:

Introduction to Semaphores and types. [2 Hrs]

Inter process communication: pipes and message box. [2 Hrs]

Revision and Test **[12 Hrs]**

TEXT BOOK:

S.No	Title	Author	Publisher with Edition
1.	Microprocessor & Microcontroller	B.P.Singa	Reprint-Galgotia Publication Pvt Ltd., - 2001
2.	Real Time Concepts for Embedded Systems	Qing Li and Caroline Yao	Elsevier publication- 2003

REFERENCE BOOKS:

S.No	Title	Author	Publisher with Edition
1.	Embedded Systems-Architecture, Programming and Design	Rajkamal	TMH, 2nd Edition-2008
2.	ARM System Developer's Guide Designing and Optimizing	Andrew N.Sloss	Elsevier publication-2004
3.	MicroC/OS – II	Jean J. Labrosse	J. Labrosse Publisher-Second Edition - 2003
4.	Embedded Systems	B.Kanta Rao	PHI publishers Eastern Economy Edition, 2011-
5.	Embedded/Real Time Systems	Dr. K.V.K.K Prasad	Curriculum Development Center – DOTE-2009
6.	ARM System- On-Chip Architecture	Steve Furbe	Second Edition - 2001

LEARNING WEBSITES

1.https://internetofthingsagenda.techtarget.com/definition/embedded-system

2.https://www.tutorialspoint.com/embedded_systems/es_overview.htm

3.https://www.elprocus.com/embedded-systems-real-time-applications/

4. https://www.edgefx.in/embedded-systems-basics-with-applications/

5.https://www.codrey.com/embedded-systems/embedded-systems-introduction/

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 610.1	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C 610.2	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C 610.3	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C 610.4	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C 610.5	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**
C 610	**15**	**10**	**10**	**10**	**15**	**10**	**15**	**10**	**15**	**15**
Correlation Level	**3**	**2**	**2**	**2**	**3**	**2**	**3**	**2**	**3**	**3**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching learning process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 620 COMPUTER HARDWARE SERVICING AND NETWORKING

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
	Hrs/Week	Hrs / Semester	Marks			Duration
			Internal Assessment	Semester End Examination	Total	
Computer Hardware Servicing and Networking	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME (Hrs)
I	Motherboard components and memory storage devices	13
II	I/O Devices and Interface	12
III	Trouble Shooting of Desktop and Laptops	12
IV	Computer Network Devices And OSI Layers	13
V	802.X and TCP/IP Protocols	13
	Revision and Test	12
	TOTAL	**75**

Course Description:

Maintaining and servicing the computers, laptops and peripherals are essential requirements of the computer students. The clear understanding of computer network devices and protocols are also taught in this subject.

OBJECTIVES:

- On completion of the following units of syllabus contents, the students can
  Identify the major components of CPU.
- Understand the principle of operations of all the interfacing boards, IO/Memory slots and interfacing devices.
- Know the use of diagnostic Software.
- Trouble shoots the problems in Laptop.
- Understand the different layers of OSI and their functions. Compare different LAN protocols.
- Identify the protocols used in TCP /IP and compare with OSI model. Use of IP addressing and TCP/ IP protocols briefly.

COURSE OUTCOMES

ECC 620 COMPUTER HARDWARE SERVICING AND NETWORKING	
After successful completion of this course, the students should be able to	
C 620.1	Explain about the Motherboard Components and Memory Storage devices of the computer .
C 620.2	Interpret about the I/O devices and interface**.**
C 620.3	Demonstrate a clear understanding of Maintenance and troubleshooting of desktop and laptops.
C 620.4	Elaborate the functions of computer network devices and OSI layers.
C 620.5	Explain about 802. X and TCP/IP protocols**.**

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ECC 620 COMPUTER HARDWARE SERVICING AND NETWORKING

UNIT I

MOTHERBOARD COMPONENTS AND MEMORY STORAGE DEVICES **[13 Hrs]**

INTRODUCTION

Hardware, Software and Firmware - Mother board, [2Hrs]

IO and memory expansion slots,

SMPS, Drives, front panel and rear panel connectors. [1Hr]

PROCESSORS

Architecture and block diagram of multicore Processor, [2Hrs]

Features of new processor(Definition only)-chipsets (Concepts only)

BUS STANDARDS

Overview and features of PCI, AGP, PCMCIA, [1Hr]

PRIMARY MEMORY

Introduction-Main Memory, Cache memory –DDR2 [2Hrs]

DDR3, – Direct RDRAM, RAM on modern computer.

SECONDARY STORAGE

Hard Disk – Construction – Working Principle – Specification [2 Hrs]

of IDE, Ultra ATA, Serial ATA

HDD Partition – Formatting.

REMOVABLE STORAGE

CD-R, CD-RW; DVD-ROM, DVD-RW [1Hr]

Construction and reading & writing operations [2Hrs]

Blue-ray: Introduction – Disc Parameters

UNIT II

I/O DEVICES AND INTERFACE **[12 Hrs]**

KEYBOARD

Keyboard – Signals – operation of membrane and mechanical keyboards - [2Hrs] Troubleshooting

Wireless keyboard. `

MOUSE

Types, connectors, operation of optical mouse and troubleshooting [1Hr]

SCANNER [1Hr]

PRINTERS

Introduction – Types of printer, Dot matrix, Inkjet, Laser, [1Hr]

MFP (Multi Function Printer) and Thermal printer - Operation – Construction –

Features and Troubleshooting

Plotter [1Hr]

I/O PORTS

Serial, Parallel, USB, Game Port, and HDMI. [1Hr]

DISPLAYS

Principles of LED, LCD and TFT Displays. [1Hr]

GRAPHIC CARDS

VGA and SVGA card. [1Hr]

MODEM

Working principles. [1Hr]

POWER SUPPLY

Servo Stabilizers, online and offline UPS – working principles; [2Hrs]

SMPS: Principles of operation and Block Diagram of ATX Power Supply,

Connector Specifications.

UNIT III

MAINTENANCE AND TROUBLE SHOOTING OF DESKTOP AND LAPTOPS [12 Hrs]

BIOS –SETUP

Standard CMOS setup, Advanced BIOS setup, Power management [1 Hr]

Advanced chipset features, PC Bios communication – upgrading BIOS,

Flash BIOS – setup [2 Hrs]

POST

Definition – IPL hardware – POST Test sequence – beep codes [2 Hrs]

DIAGNOSTIC SOFTWARE AND VIRUSES

Computer Viruses – Precautions – Anti-virus Software –identify the signature [2 Hrs]

of viruses – Firewalls and latest diagnostic software's.

LAPTOP

Types of laptop – block diagram – working principles–configuring laptops and [1 Hr]

power settings – SMD components, ESD and precautions.

LAPTOP COMPONENTS

Adapter – types, Battery – types [2 Hrs]

Laptop Mother Board - block diagram, Laptop Keyboard & Touchpad

INSTALLATION AND TROUBLESHOOTING

Formatting, Partitioning and Installation of OS – Trouble Shooting [2 Hrs]

Laptop Hardware problems – Preventive - maintenance techniques for laptops.

UNIT IV

COMPUTER NETWORK DEVICES AND OSI LAYERS **[13 Hrs]**

DATA COMMUNICATION

Components of a data communication [1Hr]

DATA FLOW

Simplex – half duplex – full duplex [1Hr]

TOPOLOGIES

Star, Bus, Ring, Mesh, Hybrid – Advantages and Disadvantages of each topology. [2 Hrs]

NETWORKS

Definition - Types of networks LAN – MAN – WAN – CAN – HAN – Internet [3 Hrs]

– Intranet –Extranet,

Client-Server, Peer To Peer Networks. [2 Hrs]

NETWORK DEVICES

Features and concepts of Switches – Routers (Wired and Wireless) – Gateways**.** [2 Hrs]

NETWORK MODELS

Protocol definition - standards - OSI Model – layered architecture – functions of [2Hrs]

all layers

UNIT V

802. X AND TCP/IP PROTOCOLS **[13 Hrs]**

OVERVIEW OF TCP / IP

TCP / IP – Transport Layers Protocol – Connection oriented and [2Hrs]

connectionless Services – Sockets – TCP & UDP

802. X PROTOCOLS

Concepts and PDU format of CSMA/CD (802.3) – Token bus (802.4) [1Hr]

– Token ring (802.5) – Ethernet – Type of Ethernet (Fast Ethernet, gigabit

Ethernet) – Comparison between 802.3, 802.4 and 802.5, [2 Hrs]

NETWORK LAYERS PROTOCOL

IP –Interior Gateway Protocols (IGMP, ICMP, ARP, RARP Concept only). [3 Hrs]

IP ADDRESSING

Dotted Decimal Notation –Subnetting & Supernetting [3 Hrs]

APPLICATION LAYER PROTOCOLS

FTP– Telnet – SMTP– HTTP – DNS – POP [2 Hrs]

Revision and Test **[12 Hrs]**

TEXT BOOKS:

Si.No	Title	Author	Publisher with Edition
1.	Computer Installation and Servicing	D.Balasubramanian	Tata McGraw Hill Publishing Company, New Delhi - 2005
2.	IBM PC and CLONES	B.Govindrajalu	Tata Mc Graw Hill Publishers, New Delhi - 2001
3.	Data Communication and networking	Behrouz A.Forouzan	Tata Mc-Graw Hill, New Delhi - 2006
4.	Computer Networks	Andrew S.Tanenbaum	Prentice-Hall of India, New Delhi - 2004

REFERENCE BOOKS:

Si.No	Title	Author	Publisher with Edition
1.	Computer Networks	Achyut Godbole	Tata Mc-Graw Hil -New Delhi - 1998
2.	Principles of Wireless Networks	A unified Approach, Kaveh Pahlavan and Prashant Krishnamurty	Pearson Education, 2002
3.	Troubleshooting, Maintaining and Repairing PCs,	Stephen J Bigelow	Tata MCGraw Hill - 2001
4.	Data and Computer Communications	William Stallings	Prentice-Hall of India, Eighth Edition - 2005
5.	Upgrading and repairing laptops	Scott Mueller	QUE Publication, Upgrading and repairing Laptops - 2004

LEARNING WEBSITES

1.http://www.depedbataan.com/resources/9/k_to_12_pc_hardware_servicing_learning_module.pdf
2.https://www.academia.edu/22093398/COMPUTER_HARDWARE_SERVICING_ICT-COMPUTER_HARDWARE_SERVICING
3.http://chs-comtipz.blogspot.com/2015/01/terms-for-computer-hardware-servicing.html
4.https://www.slideshare.net/kenjoyb/k-to-12-pc-hardware-servicing-learning-module
5. https://www.techwalla.com/articles/what-is-computer-hardware-servicing

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 620.1	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**2**	**2**	**2**
C 620.2	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**2**	**2**	**2**
C 620.3	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**2**	**2**	**2**
C 620.4	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**2**	**2**	**2**
C 620.5	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**2**	**2**	**2**
C 620	**15**	**15**	**15**	**15**	**15**	**10**	**15**	**10**	**10**	**10**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**2**	**2**	**2**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

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Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 631 TELEVISION ENGINEERING

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs/ Semester	Internal Assessment	Semester End Examination	Total	
Television Engineering	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME (Hrs)
I	Television fundamentals	14
II	Camera and picture tubes	13
III	Television transmitter	11
IV	Television receiver	13
V	Advanced television systems	12
Revision Test		12
Total		**75**

Course Description:

One of the elements of mass media communication is the television. The TV has gone with different stages of development. So the electronics engineer must be able to service the TV receiver and its attachments after knowing the working of the TV right from the transmitter from where the signal is being produced for transmission .

OBJECTIVES:

- To understand monochrome TV transmitter and receiver
- To understand principles of scanning
- To study about different TV standards
- To study fundamentals of color TV
- To learn about camera tube and its working.
- To understand the working of picture tubes monochrome
- To learn about color TV transmitter
- To know about monochrome TV Rx.
- To Study about color TV receiver .

- To know the video amplifier and HDFC
- To study fundamentals of CCTV .
- To learn HD TV and 3D TV.
- To study the telecine equipment
- To study applications of Blu ray Disk, DVD players models, USB.

COURSE OUTCOMES

ECC 631 TELEVISION ENGINEERING	
After successful completion of this course, the students should be le to	
C 631.1	Explain about monochrome and colour T.V fundamentals.
C 631.2	Elaborate about the working principle of the Camera and picture tubes.
C 631.3	Interpret the concepts of TV transmitter .
C 631.4	Explain the concepts of TV Receiver.
C 631.5	Demonstrate about advanced television systems .

.

ECC 631 TELEVISION ENGINEERING

UNIT I

TV. FUNDAMENTALS **[14 Hrs]**

Monochrome TV:

Basic block diagram of Monochrome TV transmitter and Receiver [2 Hrs]

Scanning process – horizontal ,vertical and sequential scanning [1 Hr]

flicker – interlaced scanning (qualitative treatment only) [2 Hrs]

need for synchronization – blanking pulses – Aspect ratio [1 Hr]

Resolution – Types – vertical and horizontal resolution [1 Hr]

video bandwidth – composite video signal (CVS)– CVS for one horizontal line [1 Hr]

Definitions for Vertical sync pulse, Serrated vertical pulse,

Equalizing pulse Positive & Negative modulation-TV Standards [1 Hr]

List of Types of TV standards [1 Hr]

VSB transmission and reception

COLOR T.V. FUNDAMENTALS:

Additive mixing of colours – Types [1 Hr]

color perception – Chromaticity diagram [2 Hrs]

Definition for Luminance, Hue Saturation and Chrominance Formation [1 Hr]

of chrominance signal in PAL system with weighting factors.

UNIT II

CAMERA AND PICTURE TUBES **[13 Hrs]**

CAMERA TUBE :

Characteristics of camera tube [2 Hrs]

Types of camera tube – working principle of Vidicon [2 Hrs]

Plumbicon camera tube, Newicon and Saticon Camera tube [1 Hr]

CCD camera -Video processing of camera pick up signal [2 Hrs]

Block diagram and Principle of working of colour TV camera tube.

PICTURE TUBE :

Construction and working of Monochrome picture tube [3 Hrs]

screen phosphor – screen burn – screen Persistance-

Aluminized screen- Types of color picture tubes construction and working [3 Hrs]

principle Delta gun and Trinitron colour picture tube - Automatic degaussing

UNIT III

TELEVISION TRANSMITTER	**[11 Hrs]**
Types- Comparison-Principles Block diagram of Low level	[2 Hrs]
IF Modulated TV transmitter	[2 Hrs]
Visual Exciter - Aural Exciter	[2 Hrs]
principle of working of CIN Diplexer	
Block diagram of color TV transmitter color compatibility	[2 Hrs]
PAL colour coder functional blocks and working of each block	[3 Hrs]
Merits and demerits of PAL system	
NTSC and SECAM Color Coder	

UNIT IV

TELEVISION RECEIVER	**[13 Hrs]**
Block diagram of monochrome receiver- Functions of each block	[2 Hrs]
Need for AGC- advantages of AGC	[2 Hrs]
Video amplifier requirements	[2 Hrs]
High frequency & Low frequency compensation	[2 Hrs]
Block diagram of PAL color Receiver Need for sync separator	[2 Hrs]
Basic sync separator circuits Vertical sync separation & Horizontal	
sync separation-AFC –need for AFC Horizontal AFC– Hunting in AFC-	[3 Hrs]
Anti hunt network	

UNIT V

ADVANCED TELEVISION SYSTEMS	**[12 Hrs]**
Block diagram of a digital color TV receiver	[2 Hrs]
Remote control IR transmitter and receiver - Closed circuit TV system (CCTV)	[2 Hrs]
Applications of CCTV –scrambler-necessity	
basic principle-types Descrambler block diagram Telecine equipment	[2 Hrs]
Digital CCD Telecine system	
Introduction to High definition TV(HDTV)&3DTV.	[2 Hrs]
Blue Ray Disc(BD)	
The DVD player -Block diagram-Desirable Features & outputs of DVD players	[2 Hrs]
DVD player Models - USB flash drive(pen drive).	
Television via Satellite	[2 Hrs]
Revision and Test	**[12 Hrs]**

TEXT BOOKS:

Si.No	Title	Author	Publisher with Edition
1.	Monochrome TV Practice, Principles, Technology &servicing by R.R.Gulati-Second Edition- New	R.R.Gulati	New Age Publishers - Second Edition - 2001
2.	TV & Video engg	A.M.Dhake	Tata MCGraw Hill- Second Edition-1998
3.	Monochrome & color TV	R.R.Gulati	New Age publishers -2003

REFERENCE BOOKS:

Si.No	Title	Author	Publisher with Edition
1.	Colour TV theory and practice	S.P.Bali	Tata MCGraw Hill- 1994
2.	Modern VCD- video CD player introduction, servicing and trouble shooting	Manohar latia & pradeep nair	New age publishers, second edition. - 2002

LEARNING WEBSITES

1. http://www.gcebargur.ac.in/television-and-video-engineering-notes

2. https://www.smartzworld.com/notes/subject-wise-materials/3. 3. 3.http://www.jntumaterials.com/jntuh-b-tech-r09-4-1ece-television-engineering-material-free-download/

4. https://www.technicalsymposium.com/alllecturenotes_ECE.html

5. http://www.faadooengineers.com/threads/437-TELEVISION-ENGINEERING-Ebooks-presentations-and-lecture-notes-covering-full-semester-syllabus

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 631.1	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C 631.2	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C 631.3	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C 631.4	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C 631.5	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C631 Total	**15**	**15**	**15**	**15**	**15**	**10**	**15**	**15**	**10**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

****

ECC 632 TEST ENGINEERING

TEACHING AND SCHEME OF EXAMINATION:

Number of Weeks/ Semester: 15 weeks

course	Instruction		Examination			
	Hrs/Week	Hrs / Semester	Marks			Duration
			Internal Assessment	Semester End Examination	Total	
Test Engineering	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME (Hrs)
I	Introduction to test engineering	13
II	Automated testing methods and technology	13
III	VI (Signature) testing methods and technology	13
IV	Boundary scan testing methods and technology	12
V	ATE Test Program generation & semi conductor testing	12
	Revision Test	12
	TOTAL	**75**

Course Description:

Test engineering education is in the growing stage. But every year, there is a tremendous increase in the use of modern equipment in industry therefore it is necessary for every student to understand the functioning of various equipment's. This subject to enable the students to learn the basic principles of different instruments via measurement.

A test engineer is a professional who determines how to create a process that would best test a particular product in manufacturing, quality assurance or related areas, like the RMA department, in order to assure that the product meets applicable specifications. Test engineers are also responsible for determining the best way a test can be performed in order to achieve 100% test coverage of all components using different test processes. Often test engineers also serve as a liaison between manufacturing, design engineering, sales engineering and marketing communities as well.

OBJECTIVES:

- To know the basics of introduction to test engineering
- To know about Automated Testing Methods And Technology
- vi (signature) testing methods and technology
- boundary scan testing methods and technology
- ATE test program generation & semi conductor testing

COURSE OUTCOMES

ECC 632 TEST ENGINEERING	
After successful completion of this course, the students should be able to	
C 632.1	Explain about basics of test engineering.
C 632.2	Elaborate about automated testing methods and technology.
C 632.3	Explain about the concepts of VI (signature) testing methods and technology.
C 632.4	Interpret the concepts of boundary scan testing methods and technology.
C 632.5	Explain about ATE test program generation & semi conductor .

ECC 632 TEST ENGINEERING

UNIT I

INTRODUCTION TO TEST ENGINEERING **[13 Hrs]**

Need and Importance of Test Engineering [2 Hrs]

Principles of Fundamental Testing Methods [2 Hrs]

Basic Principles of Memory Testing [2 Hrs]

PCB Track Short Testing Methods [2 Hrs]

Concepts of Trouble Shooting PCBs [3 Hrs]

Manual and Automated PCB Trouble Shooting Techniques. [2 Hrs]

UNIT II

AUTOMATED TESTING METHODS AND TECHNOLOGY **[13 Hrs]**

Introduction to Automated Test Techniques [2 Hrs]

Fundamental of Digital Logic Families [2 Hrs]

Concepts of Back-Driving / Node Forcing Technique [2 Hrs]

and its International Defense Standard

Concepts of Digital Guarding [2 Hrs]

Auto Compensation - Clock Termination

Functional Test Methods [2 Hrs]

Functional Testing of Digital, Analog and Mixed Integrated Circuit [2 Hrs]

Different types of Memory Module Functional Test. [1 Hr]

UNIT III

VI (SIGNATURE) TESTING METHODS AND TECHNOLOGY **[13 Hrs]**

Fundamentals of Electrical Characteristics [2 Hrs]

Effects of Curve Trace, Characteristics of Passive and Active Components [3 Hrs]

Understanding Composite VI-Curve and it deviations [3 Hrs]

Component Identification of Ageing Effects with VI Curve Trace, [2 Hrs]

Input and Output Characteristics of Digital Integrated Circuits [2 Hrs]

Good Versus Suspect interpretation Comparison. [1 Hr]

UNIT IV

BOUNDARY SCAN TESTING METHODS AND TECHNOLOGY **[12 Hrs]**

Introduction to Boundary Scan [2 Hrs]

Need of Boundary Scan Test Technique [2 Hrs]

Principle of Boundary Scan Test - Boundary Scan Architecture [2 Hrs]

Application of Boundary Scan Test- Boundary Scan Standards

Boundary Scan Description Language (BSDL) [2 Hrs]

Interconnect test – Serial Vector Format (SVF) Test

Basic of JTAG Port [2 Hrs]

Digital Integrated Circuit Test using Boundary Scan Techniques. [2 Hrs]

UNIT V
ATE TEST PROGRAM GENERATION & SEMI CONDUCTOR

TESTING **[12 Hrs]**

ATE in PCB Test [2 Hrs]

Test Fixtures [1 Hr]

Basics of Automatic Test Program Generation [2 Hrs]

Standard Test Data Format STDF [3 Hrs]

Basic of Digital Simulator [2 Hrs]

Introduction to Semiconductor Test, Use of Load Boards. [2 Hrs]

Revision and Test **[12 Hrs]**

TEXT BOOKS:

1. Test Engineering for Electronic Hardware – SR Sabapathi, Qmax Test Equipment's P Ltd., 2011.

REFERENCE BOOKS:

1. Practical Electronic Fault Finding and Trouble shooting by Robin Pain Newnes, Reed Educational and professional publishing Ltd., 1996.
2. The Fundamentals of Digital Semiconductor Testing, Floyd, Pearson Education India, Sep-2005.

LEARNING WEBSITES

1.https://electronicspost.com/types-of-pcb-assembly-processes/
2.https://www.iitk.ac.in/ee/data/pcb/pcb-lab.pdf 3.https://link.springer.com/article/10.1007/s00170-004-2233-1
4.https://www.compudrivesystem.com/training-division 5.http://www.trp.org.in/issues/simulation-and-implementation-of-microcontroller-based-printed-circuit-board-ready-circuits-for-technical-training-and-demonstration /

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 632.1	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C 632.2	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C 632.3	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C 632.4	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C 632.5	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**
C 632	**15**	**15**	**15**	**15**	**15**	**10**	**15**	**15**	**10**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**2**	**3**	**3**	**2**	**3**

Correlation level 1 – Slight (low)

Correlation level 2 – Moderate (Medium)

Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 633 MOBILE COMMUNICATION

TEACHING AND SCHEME OFEXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Mobile communication	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME (Hrs)
I	Introduction to Mobile Communication	13
II	Broadcast Systems	13
III	Wireless Transmission (2G)	13
IV	Wireless Networking (3G)	12
V	Mobile Network Layer & Transport Layer	12
Revision Test		12
TOTAL		**75**

Course description:

Communication is one of the integral parts of science that has always been a focus point for exchanging information among parties at locations physically apart. After its discovery, telephones have replaced the telegrams and letters. Similarly, the term ‘mobile’ has completely revolutionized the communication by opening up innovative applications that are limited to one’s imagination. Today, mobile communication has become the backbone of the society. All the mobile system technologies have improved the way of living. It’s main plus point is that it has privileged a common mass of society. In this subject, the evolution as well as the fundamental techniques of the mobile communication is discussed.

OBJECTIVES:

- To know the basics of Mobile Radio communication
- To know about wireless communications systems
- To understand the Cellular concept
- To study broadcasting
- To learn the Digital audio and video broadcasting
- To learn the convergence of mobile communications
- To know wireless communications and the process of transmission
- To study about various architectures in wireless transmission
- To study the CDMA digital standards
- To understand Mobile Services (2G), (2.5G) and (3G)
- To know the GPRS and WAP
- To learn the manufacture and operator technologies
- To learn mobile network layer & transport layer
- To study the Dynamic host configuration protocol To know the TCP &its improvements

COURSE OUTCOMES

ECC 633 MOBILE COMMUNICATION	
After successful completion of this course, the students should be able to	
C 633.1	Explain about Mobile communication and cellular concepts.
C 633.2	Explain about broadcasting techniques in mobile communications.
C 633.3	Interpret the concepts of Wireless Transmission (2G).
C 633.4	Show the knowledge on wireless networking (3G).
C 633.5	Interpret about mobile network layer and transport layer.

ECC 633 MOBILE COMMUNICATION

UNITI

INTRODUCTION TO MOBILE COMMUNICATION	**[13Hrs]**
Evolution of Mobile Radio Communication, Mobile Radio Telephony in India and around the world	[1Hr]
Examples of Wireless Communication Systems: Paging system,	[2Hrs]
Cordless telephones systems, Cellular telephone Systems, Trends in Cellular Radio and personal Communications	[2Hrs]
THE CELLULAR CONCEPT:	
Frequency reuse, Channel Assignment strategies	[2Hrs]
Hand off Strategies, Prioritizing Handoffs, Interference and system capacity,	[2Hrs]
Improving coverage and capacity in cellular systems ,Cell splitting	[2Hrs]
Sectoring, Repeaters for range extension	[2Hrs]

UNIT II

BROADCAST SYSTEMS	**[13Hrs]**
Introduction – Cyclical repetition of data –	[2Hrs]
Digital audio broadcasting –	[2Hrs]
multimedia object transfer protocol –	[2Hrs]
Digital video broadcasting –	[2Hrs]
DVB data broadcasting,	[2Hrs]
DVB for high speed internet access –	[2Hrs]
Convergence of broadcasting and mobile communications	[1Hr]

UNIT III

WIRELESS TRANSMISSION (2G)	**[13Hrs]**
Global system for mobile (GSM) - services and features –	[2Hrs]
Radio subsystem - channel types - Example of a GSM call –	[2Hrs]
Frame structure for GSM – DECT system architecture,	[2Hrs]
protocol architecture – TETRA –	[1Hr]
UMTS and IMT- 2000 - radio interface, UTRAN, core network, handover –	[3Hrs]
CDMA digital cellular standard (IS – 95): Frequency and channel specifications – Forward CDMA channel and Reverse CDMA channel	[3Hrs]

UNIT IV

WIRELESS NETWORKING (3G) **[12 Hrs]**

MOBILE SERVICES (2.5G)

GPRS: GPRS Functional groups – architecture - network nodes – [2Hrs]

Procedures - billing [1Hr]

WAP: WAP Model - WAP Gateway- WAP Protocols - WAP UA prof and

caching, wireless bearers for WAP, WAP developer tool kits – Mobile station [1Hr]

application execution environment. [1Hr]

MOBILE SERVICES (3G):

Paradigm Shifts in 3G Systems - W-CDMA and CDMA 2000 – [2Hrs]

Improvements on core network - Quality of service in 3G – [1Hr]

Wireless OS for 3G handset - 3G [1Hr]

systems and field trials - Other trail systems - Impact on manufacture and [2Hrs]

operator technologies [1Hr]

UNIT V

MOBILE NETWORK LAYER & TRANSPORT LAYER **[12 Hrs]**

Mobile IP – Goals, assumptions and requirements, Entities and terminology, [2Hrs]

IP Packet delivery, Agent discovery, Registration, tunneling and encapsulation [2Hrs]

Optimization, Reverse tunneling, IPv6, IP micro- mobility support –

Dynamic host configuration protocol – mobile ad-hoc network – routing [2Hrs]

Destination sequence distance vector – Dynamic source routing –

alternative metrics, TCP – Congestion control – slow start – [2Hrs]

fast retransmit/ fast recovery – implications of mobility – [1Hr]

Classical TCP improvements – indirect – snooping – [1Hr]

Mobile–Transmission timeout freezing – selective retransmission- [2Hrs]

Transaction oriented – TCP over 2.5/3G wireless networks –

Revision and Test **[12 Hrs]**

TEXT BOOKS :

SL.No	Title	Author	Publisher with Edition
1.	Wireless Communications Principles and Practice	Theodore S. Rappaport	Pearson Education, 2003
2.	Mobile Communications	Jochen Schiller	Pearson Education, 2009, Second edition

REFERENCE BOOKS:

SL. No	Title	Author	Publisher with Edition
1.	Wireless and Mobile Network Architectures	Yi-BingLin, Imrich Chlamtac	Wiley, 2001
2.	Mobile Cellular Communication	Gottapu Sasibhushana Rao	Pearson Education, 2012
3.	Wireless Digital Communications	Kamilo Feher	PHI, 2003
4.	Mobile Cellular Communications	W.C.Y. Lee	2nd Edition, MC Graw Hill, 1995
5.	Wireless Networks	P. Nicopolitidis	Wiley, 2003
6.	Wireless Communications and Networks	William Stallings	2nd Edition,Prentice Hall of India-2006

LEARNING WEBSITES

1. https://www.javatpoint.com/mobile-communication-introduction
2. https://electronicsforu.com/technology-trends/mobile-communication-1g-4g
3. https://www.electroschematics.com/5231/mobile-phone-how-it-works/
4. https://www.igi-lobal.com/dictionary/communicame/34130
5. https://www.tutorialspoint.com/umts/umts_history_of_mobile_communication.htm

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 633.1	3	3	3	3	3	2	3	3	2	3
C 633.2	3	3	3	3	3	2	3	3	2	3
C 633.3	3	3	3	3	3	2	3	3	2	3
C 633.4	3	3	3	3	3	2	3	3	2	3
C 633.5	3	3	3	3	3	2	3	3	2	3
C 633	15	15	15	15	15	10	15	15	10	15
Correlation Level	3	3	3	3	3	2	3	3	2	3

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 640 EMBEDDED SYSTEMS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

No of weeks per semester: 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Embedded systems practical	4	60	25	75	100	3 Hrs

ALLOCATION OF MARKS

Title	Marks
Algorithm/flow chart	15
Program	25
Execution	20
Result	10
Viva	5
Total	75

Course description

ARM is a major processor widely used in the embedded system in products ranging from cell/mobile phones to automotive braking and control systems. Since 1985, the ARM architecture has become the most pervasive 32-bit architecture in the world. This practical course has been set up to describe the operation of the ARM core from experimenting simple exercises with a clear emphasis on its architecture by assuming no previous ARM experience. In Diploma level, the ARM architecture is studied and experimented for its internals through hands on. This is achieved by experiencing the experiments through industrial and society describe the system requirement and to make a complete prototype working model.

LIST OF EQUIPMENTS AND REQUIREMENTS:

1. ARM7 TDMI Kit – 10 nos with interface boards for the above experiments The Chip set may be TMS470, LPC2138, LPC2148, or STR7 etc
2. Interfaces:RTC, ADC, LCD, Seven segment display, LEDS and Switches.
3. Manual for the kit and for interfacing board with stepper motor
4. Manual for the built in function for the Board

OBJECTIVES:

On completion of the following exercises, the students must be able to

- To study the Processor kit
- To develop and executed an assembly level program
- To realizing the timer peripheral in ARM by using :polling and interrupt driven method
- To develop and realize the ASM
- To access the programs by using LCD in ARM processor
- To interface stepper motor in ARM processor
- To implement, creating and Deleting the task by using RTOS.

COURSE OUTCOMES

ECC 640 EMBEDDED SYSTEMS PRATICAL	
After successful completion of this course, the students should be able to	
C 640.1	Explain about ARM processor kit and simulate arithmetic operation, soft delay and LED blinking with variable speed.
C 640.2	Develop the input and output port in ARM **,**timer peripheral in ARM by polling method and timer peripheral in ARM by interrupt driven method.
C 640.3	Develop C Program and execute serial transmission and reception of a character by interrupt method, displaying alphanumeric characters in 2x16 line LCD module.
C 640.4	Develop the program for converting hexadecimal to decimal and to display in LCD.
C 640.5	Elaborate the Interfacing the stepper motor in ARM processor and generation of PWM

ECC 640 EMBEDDED SYSTEMS PRACTICAL

S.No	Name of the experiment	Course Outcome
1	**STUDY OF ARM PROCESSOR KIT** (whatever the ARM processor kit the institution is having) Example: LPC2148 The student should able to Understand the memory mapping of the IO and peripherals List the peripherals present in the processor Explain that how to use an IO pin, related SFRs and instructions Explain that how to use timer, UART, its related SFR and instructions sets	**C 640.1**
2	**SIMULATION OF ARITHMETIC OPERATION ON ARM IN ASSEMBLY** Develop an assembly level code for the single precision (32 bit) arithmetic function. a. Addition, b. Subtraction and b. Multiplication (Note: simulate the program in the software)	**C 640.1**
3	**SIMULATION OF ASSEMBLY LEVEL PROGRAM FOR SOFT DELAY** Develop an assembly level code for the 32 bit or 64 bit delay routine. Calculate the no of clock taken for the routine and adjust the delay value for the desired. (Note: simulate the program in the software)	**C 640.1**
4	**SIMPLE LED BLINKING WITH VARIABLE SPEED IN ASM** Develop an assembly level program of ARM processor to blink a LED (including delay routine) in variable speed in the trainer kit. Upon change in the delay program the speed should vary. No need to change the speed dynamically. (Note: Student should study the list of special function registers associated for accessing the IO pin. Manual containing List of IO registers (SFR for IO) can be given to the students for the final exam)	**C 640.1**
5	**REALIZATION OF INPUT AND OUTPUT PORT IN ASM** Develop an assembly level program of ARM processor to read a port in which switches are connected in the trainer kit. Send back the receive input to output in which LEDs are connected in the trainer kit Note: Student should study the list of special function registers associated for accessing Port the read and write. Manual containing List of IO registers (SFR for IO) can be given to the students for the board exam)	**C 640.2**
6	**SIMPLE LED BLINKING WITH VARIABLE SPEED IN C** Develop a C program for ARM processor to blink a LED (including delay routine) in variable speed. Upon change in the input switch the speed should vary. (Note: The C code should be in while loop)	**C 640.2**
7	**SEVEN SEGMENT LED DISPLAY INTERFACE IN C** Develop a C program for ARM processor to interface a seven segment LED display. The display should count up for every one second.	**C 640.2**
8	**SEVEN SEGMENT LED DISPLAY INTERFACE IN C** Develop a C program for ARM processor to interface a seven segment LED display. The display should count up for every one second. The delay can be used from experiment.	**C 640.2**
9	**REALIZING TIMER PERIPHERAL IN ARM BY POLLINGMETHOD** Develop a C program for ARM processor to run a timer peripheral in ARM. The timer flag can be pooled for timer end. As timer ends reset the timer and update new value to the LED display.	**C 640.1**

10	**REALIZING TIMER PERIPHERAL IN ARM BY INTERRUPT DRIVEN METHOD** Develop a C program for ARM processor to run a timer peripheral in ARM. The timer flag can be pooled for timer end. As timer ends reset the timer and update new value to the LED display.	**C 640.2**
11	**SERIAL TRANSMISSION AND RECEPTION OF A CHARACTER IN C BY POLLING METHOD** Write a C Programs for receiving a character from other device (Computer) and send the next character of the received one to the device back. Note: Student should understand the SFRs used for serial communication. Manual containing list of SFRs for the UART can be given to the students for their final examination	**C 640.2**
12	**SERIAL TRANSMISSION AND RECEPTION OF A CHARACTER IN C BY INTERRUPT METHOD** Write a C Programs for receiving a character from other device (Computer) and send the next character of the received one to the device back.	**C 640.3**
13	**DISPLAYING ALPHANUMERIC CHARACTERS IN 2X16 LINE LCD MODULE** Write a C Programs for displaying a number and an alphabet in the LCD module by just calling the built in LCD function. The display should come in the desired line and column. (Built in function for the LCD can be given in the manual)	**C 640.3**
14	**CONVERTING HEXADECIMAL TO DECIMAL AND TO DISPLAY IN LCD** Write a C Programs for converting the given 8 bit hexadecimal into decimal and there by converting into ASCII which is to be displayed in the LCD module. (Built in function for the LCD can be given in the manual)	**C 640.4**
15	**ACCESSING INTERNAL ADC OF THE ARM PROCESSOR AND TO DISPLAY IN LCD** Write a C Program for reading an ADC, convert into decimal and to display it The ADC input is connected to any analog sensor. (Note: Student should study the SFR associated with ADC, Manual containing List of SFR for accessing ADC can be given for the examination.)	**C 640.4**
16	**ACCESSING INTERNAL ADC OF THE ARM PROCESSOR AND TO DISPLAY IN LCD** Write a C Program for reading an ADC, convert into decimal and to display it The ADC input is connected to any analog sensor. (Note: Student should study the SFR associated with ADC, Manual containing List of SFR for accessing ADC can be given for the examination.)	**C 640.4**
17	**INTERFACING STEPPER MOTOR IN ARM PROCESSOR** Write a C programs for running stepper motor either in clock wise or counter clock wise.A switch used for selecting the direction of the rotation. (Note: students should study the SFR associated with RTC, Manual containing list of SFR for accessing RTC can be given for the examination)	**C 640.5**
18	**GENERATION OF PWM** Write C program to generate a PWM signal	**C 640.5**

Learning websites

https://www.slideshare.net/nirajbharambe/embedded-system-practical-manual-1

https://muresults.net/itacademic/Workshopdata/ES.pdf

http://www.inf.ed.ac.uk/teaching/courses/es/PDFs/Coursework-2.pdf

http://www.inf.ed.ac.u

https://www.researchgate.net/publication/272485567_Practical_Aspects_of_Embedded_System_Design_using_Microcontrollersk/teaching/courses/es/PDFs/Coursework-2.pdf

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

p) Attendance : 5 marks – (Award of marks same as theory subjects)

q) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

r) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 640.1	3	3	3	3	3	3	3	2	3	3
C 640.2	3	3	3	3	3	3	3	2	3	3
C 640.3	3	3	3	3	3	3	3	2	3	3
C 640.4	3	3	3	3	3	3	3	2	3	3
C 640.5	3	3	3	3	3	3	3	2	3	3
C 640	15	15	15	15	15	15	15	10	15	15
Correlation Level	3	3	3	3	3	3	3	2	3	3

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

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ECC 650 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester: 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Computer Hardware Servicing and Networking Practical	4	60	25	75	100	3 Hrs

ALLOCATION OF MARKS:

CONTENT	MAX. MARKS	
	PART - A	PART - B
Procedure	15	15
Execution	15	15
Result with printout	5	5
Viva	5	
Total	75	

Course Description

The course aims at making the students familiar with various parts of computers and laptops and how to assemble them and the different types of peripherals desired. In addition, the course will provide the students with necessary knowledge and skills in computer and laptop software installation and maintenance and to make him diagnose the software faults. This subject also gives the knowledge and competency to diagnose systematic repair and maintenance of computers and laptops

HARDWARE REQUIREMENTS :

Computer with Pentium / Core processors with inbuilt NIC -30 Nos

Hard disk drive -02 Nos

CDD/ DVD Writer -02 Nos

Blank Blu-ray disk -30 Nos

Web camera -02 Nos

Laser Printer -02 Nos

Dot matrix Printer -02 Nos

Blank DVD -30 Nos

Scanner -02 Nos

Laptop -02 Nos

Bio metric device -02 Nos

Crimping Tool -06 Nos

Network Cables

RJ45 Tester -06 Nos

Modem with internet connection -02 Nos

Hub -02 Nos

Switch/ Router -02 Nos

SOFTWARE REQUIREMENTS:

Windows XP operating system/ Windows 7 OS

DVD/ CD Burning S/W (Ahead Nero or latest S/W)

OBJECTIVES

- On completion of the following exercises, the students must be able to
- Know the various indicators, switches and connectors used in Computers.
- Familiarize the layout of SMPS, motherboard and various Disk Drives.
- Configure Bios set up options.
- Install various secondary storage devices with memory partition and formatting.
- Know the various types of printer installation and to handle the troubleshooting ability.
- Acquire the practical knowledge about the installation of various devices like scanner, web camera, cell phone and bio-metric devices.
- Assemble PC system and checking the working condition.

COURSE OUTCOMES

ECC 650 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL	
After successful completion of this course, the students should be able to	
C650.1	Identify the system layout, installation of hard disk and DVD/BLU-ray writer
C650.2	Explain the Installation and configuring printer, Scanner , Web cam and bio-metric device
C650.3	Demonstrate the Installation OS and Dual OS in the assembled system and assemble and disassemble a Laptop to identify the parts and install OS in the laptop.
C650.4	Demonstrate the Cabling works for establishing a network ,Crimp the network cable with RJ 45 connector and test the crimped cable using a cable tester and interface two PCs to form Peer To Peer network using the connectivity devices Switch or Router in a LAN .
C650.5	Interpret the Sharing of the files,folders, printer in a LAN, Configure DNS, Install and configure Network Devices: HUB,Switch or Routers, Install and configure a DHCP server and Connect the computer in local area network.

ECC 650 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL

S. No	Name of the experiment	Course Outcome
1	**PART A – COMPUTER HARDWARE SERVICING** **IDENTIFICATION OF SYSTEM LAYOUT** i) Identify front panel indicators & switches and Front side & rear side connectors ii) Familiarize the computer system layout by marking positions of SMPS, Motherboard, FDD, HDD, CD, DVD and add on cards.	**C650.1**
2	**HARD DISK** i) Configure bios setup program and troubleshoot the typical problems using BIOS utility. ii) Install, Configure, Partition and Format Hard disk.	**C650.1**
3	**DVD/BLU-RAY WRITER** i) Install and Configure a DVD Writer and record a blank DVD. ii) Install and Configure a Blu-ray Writer and record a blank Blu-ray Disc.	**C650.1**
4	**Printer Installation** i) Install and configure Dot matrix printer ii) Install and configure Laser printer	**C650.2**
5	i) Install and configure Scanner ii) Install and configure Web cam and bio-metric device	**C650.2**
6	i) Assemble a system with add on cards and check the working condition of the system ii) Install OS in the assembled system.	**C650.3**
7	Install Dual OS in a system	**C650.3**
8	i) Assemble and Disassemble a Laptop to identify the parts. ii) Install OS in the laptop.	**C650.3**
9	**PART B – COMPUTER NETWORKING** Do the following Cabling works for establishing a network i) Crimp the network cable with RJ 45 connector in Standard cabling mode and cross cabling mode. ii) Test the crimped cable using a cable tester.	**C650.4**
10	Use IPCONFIG, PING , TRACERT and NETSTAT utilities to debug the network issues.	**C650.4**
11	Interface two PCs to form Peer To Peer network using the connectivity devices Switch or Router in a LAN .	**C650.4**
12	Share the files and folders in a LAN.	**C650.5**
13	Share a printer in a LAN.	**C650.5**
14	Configure DNS to establish interconnection between systems and describe how a name is mapped to IP Address	**C650.5**
15	i) Install and configure Network Devices: HUB, Switch or Routers ii) Install and Configure NIC.	**C650.5**
16	Install and configure a DHCP server in windows with IP address ranging from 192.168.1.1 to 192.168.1.100 and configure a DHCP client	**C650.5**
17	Connect the computer in local area network.	**C650.5**

Learning websites

https://www.academia.edu/22093398/COMPUTER_HARDWARE_SERVICING_ICT-COMPUTER_HARDWARE_SERVICING

http://chs-comtipz.blogspot.com/2015/01/terms-for-computer-hardware-servicing.html

https://www.finduniversity.ph/majors/computer-hardware-servicing-2-philippines/

https://www.nvtighana.org/pdf/SYLLABUS/COMPUTER%20HARDWARE.pdf

http://tesda3.com.ph/-downloads/TR-Computer-Hardware-Servicing-NC-II.doc

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

a) Attendance : 5 marks – (Award of marks same as theory subjects)

b) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

c) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

level 1 – (low)

level 2 –

level 3 – (high)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C650.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**2**	**3**
C650.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**2**	**3**
C650.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**2**	**3**
C650.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**2**	**3**
C650.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**2**	**3**
C650	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**10**	**10**	**15**
Correlation level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**	**2**	**3**

Correlation Slight

Correlation Moderate (Medium)

Correlation Substantial

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ECC 660 ADVANCED MICROCONTROLLER AND SIMULATION PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester : 15 weeks

Course	Instruction		Examination			
			Marks			
	Hrs/Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	Duration
Simulation Practical	4	60	25	75	100	3 Hrs

ALLOCATION OF MARKS

I) Program / Circuit Design	– 25 Marks
II) Execution	– 25 Marks
III) Result	– 20 Marks
IV) Viva – Voice	– 5 Marks

TOTAL	**75 Marks**

Course Description

To design and verify the results of various electronic circuits using simulation software and verify the result in the computer. Today engineering field has developed to a great extent that there is always the need for study of various simulation concepts for doing the experiments instead of doing the experiments in laboratory. This lab is fulfill the need for students to study the simulation software and able to design the various Electronic circuits like Rectifier circuits, Waveform Generator, Single side & Multilayer PCB layout.

OBJECTIVES

At the end of the course , the students will be able to,

- Design the Rectifier circuits like Half wave, Full wave & Bridge rectifiers with filters.
- Design a Power Supply with Regulators.
- Construct the Waveform Generator using transistors
- Design the circuits for Clipper & Clamper, Op-am applications, Instrumentation amplifiers.
- Design the Modulation & Demodulation circuits like AM,FM, ASK,FSK,PSK.
- Design the Single side & Multilayer PCB layout using CAD tool
- Design the ATMEGA2560 advanced microcontroller Kit with simple programmes.

COURSE OUTCOMES

ECC 660 ADVANCED MICROCONTROLLER AND SIMULATION PRACTICAL	
After successful completion of this course, the students should be able to	
C660.1	Explain about ATMEGA2560 advanced microcontroller Kit **.**
C660.2	Develop and implement the program for moving the robot , white line follower, obstacle avoidance with buzzer indication,2x16 LCD interface for welcome display
C660.3	Design the Simulating circuits of Rectifier circuits (Half wave, Full wave & Bridge rectifiers with filters) Astable multivibrators and monostable multivibrators .
C660.4	Design the Simulating circuits of the Clippers & Clampers, Op-amp Application, Instrumentation amplifiers
C660.5	Design the Simulating circuits of the AM , FM, ASK ,FSK , PSK Modulation and Demodulation circuits.

ECC 660 ADVANCED MICROCONTROLLER AND SIMULATION PRACTICAL

S.No	Name of the experiment	Course Outcome
1	Study of ATMEGA2560 advanced microcontroller Kit	C660.1
2	Develop and implement the program for moving the robot in forward and backward direction using ATMEGA2560 microcontroller	C660.2
3	Develop the program for white line follower robot using ATMEGA2560 microcontroller.	C660.2
4	Develop the program for obstacle avoidance with buzzer indication using ATMEGA2560 microcontroller.	C660.2
5	Develop the program for obstacle avoidance with buzzer indication using ATMEGA2560 microcontroller.	C660.2
6	Develop the program for 2x16 LCD interface for welcome display using ATMEGA2560 microcontroller.	C660.2
7	SIMULATION PRACTICAL Note : All experiments should be designed and verified through SPICE simulation tool (like PSPICE/Multisim/Lab VIEW/OrCAD/TINA) Rectifier circuits (Half wave, Full wave & Bridge rectifiers with filters)	C660.3
8	Power supply design with regulators (Astable multivibrators)	C660.3
9	Waveform generators using transistors (Astable multivibrators)	C660.3
10	Waveform generators using transistors (monostable multivibrators)	C660.3
11	Clippers & Clampers.	C660.4
12	Op-amp Application – I (any three circuits) (Inverting and non-inverting amplifiers, Voltage follower, Integrator, Differentiator, Summing amplifier, Difference amplifier)	C660.4
13	Instrumentation amplifiers	C660.4
14	AM Modulation and Demodulation	C660.5
15	FM Modulation and Demodulation	C660.5
16	ASK Modulation and Demodulation	C660.5
17	FSK Modulation and Demodulation	C660.5
18	PSK Modulation and Demodulation	C660.5

Learning websites

1.https://www.mhlnews.com/technology-amp-automation/practical-sim 2.https://e

https://www.josoorinstitute.qa/education-3.development/courses/Practical-

4.Simulationn.wikipedia.org/wiki/Computer_simulationulation

5.https://www.sciencedirect.com/science/article/pii/S0734242X83710153

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

a) Attendance : 5 marks – (Award of marks same as theory subjects)

b) Procedure/ observation and tabulation/

Other Practical related work : 10 marks

c) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C660.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

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ECC 670 PROJECT WORK

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester : 15 weeks

course	Instruction		Examination			
	Hrs/Week	Hrs / Semester	Marks			Duration
			Internal Assessment	Semester End Examination	Total	
Project Work	5	75	25	75	100	3 Hrs

OBJECTIVES:

- The project is aimed to assemble test a photo type model of any one item/gadget
- Real time application problems if any may be identified from any industry and maybe chosen
- The knowledge and the skill so far acquired may be made use of.
- The team spirit may be motivated
- The entrepreneurship ideas may be motivated by conducting a career guidance programme
- Learn and understand the gap between the technological knowledge acquired through curriculam and the actual industrial need and to compense it by acquiring additional knowledge as required.

Detail of Assessment	Period of Assessment	Max. Marks
First Review	6 th week	10
Second Review	15 th week	10
Attendance	Entire semester	5
Total		25

COURSE OUTCOMES

ECC 670 PROJECT WORK	
After successful completion of this course, the students should be able to	
C670.1	Identify Real time application problems and apply the acquired knowledge and skills to solve it.
C670.2	Design ,assemble and test a proto type model.
C670.3	Show the team spirit and get motivated.
C670.4	Develop the entrepreneurship ideas through career guidance programme
C670.5	Analyze the gap between the technological knowledge acquired through curriculum and the actual industrial needs and to compensate it by acquiring additional knowledge as required.

EVALUATION FOR AUTONOMOUS EXAMINATION:

PROJECT WORK

The Students of all the Diploma courses have to do a Project Work as part of the Curriculum and in Partial fulfillment for the award of Diploma by the State Board of Technical Education and Training, Tamil Nadu. In order to encourage students to do worthwhile and innovative projects, every year prizes are awarded for the best three projects i.e. institution wise, region wise and state wise. **The Project work must be reviewed twice in the same semester.**

c) Internal Assessment Mark for Project Work & Viva Voce

Project Review I	:	10 Marks
Project Review II	:	10 marks
Attendance	:	05 marks (Award of marks same as theory subject pattern)
Total	**:**	**25 marks**

Proper record to be maintained for the two project reviews, and it should be preserved for 2 semesters and produced to the flying squad and the inspection team at the time of inspection/ verification.

Allocation of Marks for project work & Viva Voce in Autonomous Examination

Viva Voce	:	30 marks
Marks for Report Preparation & Demo	:	35 marks
Total	**:**	**65 marks**

d) Written Test Mark (from 2 topics for 30 minutes duration) #

iii)	Environment Management	2 questions x 2 ½ marks	= 5 marks
iv)	Disaster Management	2 questions x 2 ½ marks	= 5 marks
			10 marks

Selection of questions should be from Question Bank, by the External Examiner, No Choice need be given to the candidates

Project Work & Viva Voce in Autonomous Examination	- 65 Marks
Written Test Mark (from 2 topics for 30 minutes duration)	- 10 Marks
Total	**75 marks**

A neatly prepared PROJECT REPORT as per the format has to be submitted by individual student during the project Work & Viva voce Autonomous Examination.

DETAILED SYLLABUS

ENVIRONMENTAL & DISASTER MANAGEMENT

1. ENVIRONMENTAL MANAGEMENT Introduction – Environmental Ethics – Assessment of Socio Economic Impact – Environmental Audit – Mitigation of adverse impact on Environment – Importance of Pollution Control – Types of Industries and Industrial Pollution.

Solid waste management – Characteristics of Industrial wastes – Methods of Collection, transfer and disposal of solid wastes – Converting waste to energy – Hazardous waste management Treatment technologies.

Waste water management – Characteristics of Industrial effluents – Treatment and disposal methods – Pollution of water sources and effects on human health.

Air pollution management – Sources and effects – Dispersion of air pollutants – Air pollution control methods – Air quality management.

Noise pollution management – Effects of noise on people – Noise control methods.

2. DISASTER MANAGEMENT Introduction – Disasters due to natural calamities such as Earthquake, Rain, Flood, Hurricane, Cyclones etc – Man made Disasters – Crisis due to fires, accidents, strikes etc – Loss of property and life..

Disaster Mitigation measures – Causes for major disasters – Risk Identification – Hazard Zones – Selection of sites for Industries and residential buildings – Minimum distances from Sea – Orientation of Buildings – Stability of Structures – Fire escapes in buildings - Cyclone shelters – Warning systems.

Disaster Management – Preparedness, Response, Recovery – Arrangements to be made in the industries / factories and buildings – Mobilization of Emergency Services - Search and Rescue operations – First Aids – Transportation of affected people – Hospital facilities – Fire fighting arrangements – Communication systems – Restoration of Power supply – Getting assistance of neighbors / Other organizations in Recovery and Rebuilding works – Financial commitments – Compensations to be paid – Insurances – Rehabilitation.

LIST OF QUESTIONS

1. ENVIRONMENTRAL MANAGEMENT

1. What is the responsibility of an Engineer-in-charge of an Industry with respect to Public Health?
2. Define Environmental Ethic.
3. How Industries play their role in polluting the environment?
4. What is the necessity of pollution control? What are all the different organizations you know, which deal with pollution control?
5. List out the different types of pollutions caused by a Chemical / Textile / Leather / Automobile / Cement factory.
6. What is meant by Hazardous waste?
7. Define Industrial waste management.
8. Differentiate between garbage, rubbish, refuse and trash based on their composition and source.
9. Explain briefly how the quantity of solid waste generated in an industry could be reduced.
10. What are the objectives of treatments of solid wastes before disposal?
11. What are the different methods of disposal of solid wastes?
12. Explain how the principle of recycling could be applied in the process of waste minimization.
13. Define the term 'Environmental Waste Audit'.
14. List and discuss the factors pertinent to the selection of landfill site.
15. Explain the purpose of daily cover in a sanitary landfill and state the minimum desirable depth of daily cover.
16. Describe any two methods of converting waste into energy.
17. What actions, a local body such as a municipality could take when the agency appointed for collecting and disposing the solid wastes fails to do the work continuously for number of days?
18. Write a note on Characteristics of hazardous waste.
19. What is the difference between municipal and industrial effluent ?
20. List few of the undesirable parameters / pollutants anticipated in the effluents from oil refinery industry / thermal power plants / textile industries / woolen mills / dye industries / electroplating industries / cement plants / leather industries (any two may be asked)
21. Explain briefly the process of Equalization and Neutralization of waste water of varying characteristics discharged from an Industry.
22. Explain briefly the Physical treatments "Sedimentation" and "Floatation" processes in the waste water treatment.
23. Explain briefly when and how chemical / biological treatments are given to the waste water.
24. List the four common advanced waste water treatment processes and the pollutants they remove.
25. Describe refractory organics and the method used to remove them from the effluent.
26. Explain biological nitrification and de-nitrification.
27. Describe the basic approaches to land treatment of Industrial Effluent.
28. Describe the locations for the ultimate disposal of sludge and the treatment steps needed prior to ultimate disposal.
29. List any five Industries, which act as the major sources for Hazardous Air Pollutants.

30. List out the names of any three hazardous air pollutants and their effects on human health.
31. Explain the influence of moisture, temperature and sunlight on the severity of air pollution effects on materials.
32. Differentiate between acute and chronic health effects from Air pollution.
33. Define the term Acid rain and explain how it occurs.
34. Discuss briefly the causes for global warming and its consequences
35. Suggest suitable Air pollution control devices for a few pollutants and sources.
36. Explain how evaporative emissions and exhaust emissions are commonly controlled.
37. What are the harmful elements present in the automobile smokes? How their presence could be controlled?
38. What is the Advantage of Ozone layer in the atmosphere? State few reasons for its destruction.
39. Explain the mechanism by which hearing damage occurs.
40. List any five effects of noise other than hearing damage.
41. Explain why impulsive noise is more dangerous than steady state noise.
42. Explain briefly the Source – Path – Receiver concept of Noise control.
43. Where silencers or mufflers are used ? Explain how they reduce the noise.
44. Describe two techniques to protect the receiver from hearing loss when design / redress for noise control fail.
45. What are the problems faced by the people residing along the side of a railway track and near to an Airport? What provisions could be made in their houses to reduce the problem?

2. DISASTER MANAGEMENT

1. What is meant by Disaster Management? What are the different stages of Disaster management?
2. Differentiate Natural Disasters and Man made Disasters with examples.
3. Describe the necessity of Risk identification and Assessment Surveys while planning a project.
4. What is Disasters recovery and what does it mean to an Industry?
5. What are the factors to be considered while planning the rebuilding works after a major disaster due to flood / cyclone / earthquake? (Any one may be asked)
6. List out the public emergency services available in the state, which could be approached for help during a natural disaster.
7. Specify the role played by an Engineer in the process of Disaster management.
8. What is the cause for Earthquakes? How they are measured? Which parts of India are more vulnerable for frequent earthquakes?
9. What was the cause for the Tsunami 2004 which inflicted heavy loss to life and property along the coast of Tamilnadu ? Specify its epicenter and magnitude.
10. Specify the Earthquake Hazard Zones in which the following towns of Tamilnadu lie: (a) Chennai (b) Nagapattinam (c) Coimbatore (d) Madurai (e) Salem.
11. Which parts of India are experiencing frequent natural calamities such as (a) heavy rain fall (b) huge losses due to floods (c) severe cyclones
12. Define basic wind speed. What will be the peak wind speed in (a) Very high damage risk zone – A, (b) High damage risk zone, (c) Low damage risk zone.
13. Specify the minimum distance from the Sea shore and minimum height above the mean sea level, desirable for the location of buildings.
14. Explain how the topography of the site plays a role in the disasters caused by floods and cyclones.

15. Explain how the shape and orientation of buildings could reduce the damages due to cyclones.
16. What is a cyclone shelter ? When and where it is provided ? What are its requirements ?
17. What Precautionary measures have to be taken by the authorities before opening a dam for discharging the excess water into a canal/river ?
18. What are the causes for fire accidents ? Specify the remedial measures to be taken in buildings to avoid fire accidents.
19. What is a fire escape in multistoried buildings ? What are its requirements ?
20. How the imamates of a multistory building are to be evacuted in the event of a fire/Chemical spill/Toxic Air Situation/ Terrorist attack, (any one may be asked).
21. Describe different fire fighting arrangements to be provided in an Industry.
22. Explain the necessity of disaster warning systems in Industries.
23. Explain how rescue operations have to be carried out in the case of collapse of buildings due to earthquake / blast / Cyclone / flood.
24. What are the necessary steps to be taken to avoid dangerous epidemics after a flood disaster?
25. What relief works that have to be carried out to save the lives of workers when the factory area is suddenly affected by a dangerous gas leak / sudden flooding ?
26. What are the difficulties faced by an Industry when there is a sudden power failure? How such a situation could be managed?
27. What are the difficulties faced by the Management when there is a group clash between the workers? How such a situation could be managed?
28. What will be the problems faced by the management of an Industry when a worker dies because of the failure of a mechanical device due to poor maintenance? How to manage such a situation ?
29. What precautionary measures have to be taken to avoid accidents to labourers in the Industry in a workshop / during handling of dangerous Chemicals / during construction of buildings / during the building maintenance works.
30. Explain the necessity of medical care facilities in an Industry / Project site.
31. Explain the necessity of proper training to the employees of Industries dealing with hazardous products, to act during disasters.
32. What type of disaster is expected in coal mines, cotton mills, Oil refineries, ship yards and gas plants?
33. What is meant by Emergency Plan Rehearsal? What are the advantages of such Rehearsals?
34. What action you will take when your employees could not reach the factory site because of continuous strike by Public Transport workers?
35. What immediate actions you will initiate when the quarters of your factory workers are suddenly flooded due to the breach in a nearly lake / dam, during heavy rain?
36. What steps you will take to avoid a break down when the workers union of your Industry have given a strike notice?
37. List out few possible crisis in an organization caused by its workers? What could be the part of the middle level officials in managing such crisis?
38. What types of warning systems are available to alert the people in the case of predicted disasters, such as floods, cyclone etc.
39. Explain the necessity of Team work in the crisis management in an Industry / Local body.

40. What factors are to be considered while fixing compensation to the workers in the case of severe accidents causing disability / death to them?
41. Explain the legal / financial problems the management has to face if safely measures taken by them are found to be in adequate.
42. Describe the importance of insurance to men and machinery of an Industry dealing with dangerous jobs.
43. What precautions have to be taken while storing explosives in a match/ fire crackers factory?
44. What are the arrangements required for emergency rescue works in the case of Atomic Power Plants?
45. Why residential quarters are not constructed nearer to Atomic Power Plants?

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C670.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

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ECC 610 EMBEDDED SYSTEMS
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
1.	What is the function of interrupt controller?	II	U
2.	Define endianness.	I	R
3.	What is the use of data processing instructions?	II	U
4.	Explain stack and stack pointer.	II	R
5.	What is cache hit & cache miss?	III	U
6.	What is wake up timer?	IV	R
7.	Define multitasking.	V	R
8.	Define context switching.	V	R
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
9.	Compare RISC and CISC.	I	An
10.	Write ALP for multiplication.	II	U
11.	Write about data processing instructions supported by ARM.	II	U
12.	Draw the cache architecture and explain.	III	R
13.	Explain UART in detail.	IV	U
14.	Explain flushing of a ARM cache core.	III	U
15.	Explain SLOS in detail.	V	U
16.	What is the purpose of I^2C Interface?	IV	R

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's level**	**Max marks**
17.	**A.**	Explain embedded hardware with neat diagram.	I	U	10
		(OR)			
	B.	Explain ARM design philosophy and development tools.	I	U	10
18	**A.**	Explain Memory management unit with neat block diagram.	II	U	10
		(OR)			
	B.	Explain Cache architecture and cache policies.	II	U	10
19.	**A.**	Explain thump instruction set and load – store instruction set.	III	R	10
		(OR)			
	B.	Explain Interrupts, and IRQ / FIQ exceptions interrupt.	III	R	10
20.	**A.**	Explain Universal Asynchronous Receiver/Transmitter.	IV	U	10
		(OR)			
	B.	Explain General Purpose Input/Output.	IV	U	10
21.	**A.**	Explain Simple Little Operating System.	V	U	10
		(OR)			
	B.	Explain Real-time operating systems.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 620 COMPUTER HARDWARE SERVICING AND NETWORKING
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
1.	What is a Chipset?	I	U
2.	Define: BUS.	I	R
3.	What is the use of ultra ATA?	I	U
4.	What is Blue ray?	I	U
5.	Expand the term LED.	II	R
6.	What is parallel port?	II	R
7.	Expand the term UPS.	II	R
8.	List out the types of printers.	II	U
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
9.	Define: BIOS.	III	R
10.	List out the types of adapter.	III	R
11.	Give the types of RAM.	I	R
12.	Expand POST	III	R
13.	What is half duplex?	IV	U
14.	Give any two advantages of star topology.	IV	U
15.	Expand the term MAN.	IV	R
16.	What are the types of transmission media?	IV	R

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's level**	**Max marks**
17.	**A.**	Explain architecture and block diagram of multicore Processor.	I	U	10
		(OR)			
	B.	Explain hard disk construction and working principle with neat diagram.	I	U	10
18	**A.**	Explain working principle of modem with neat diagram.	II	U	10
		(OR)			
	B.	Explain working principle of SMPS with neat diagram.	II	U	10
19.	**A.**	Explain block diagram of laptop motherboard with neat diagram.	III	AP	10
		(OR)			
	B.	Explain Formatting, Partitioning and Installation of OS.	III	U	10
20.	**A.**	Explain different types of network with neat diagram.	IV	U	10
		(OR)			
	B.	Explain different types of topology with neat diagram.	IV	AP	10
21.	**A.**	Explain Dotted Decimal Notation, Subnetting & Supernetting.	V	An	10
		(OR)			
	B.	Explain TCP/IP protocol.	V	An	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 631 TELEVISION ENGINEERING
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
1.	What is scanning?	I	R
2.	What is meant by flicker?	I	R
3.	Mention any two TV standards	I	R
4.	What is the need for synchronizing pulses?	I	R
5.	Mention the types of camera tube	II	R
6.	What is automatic degaussing?	II	R
7.	Define screen burn	II	R
8.	What is meant by dark current?	II	R
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
9.	What is high level modulation?	III	R
10.	What is the use of visual exciter?	III	R
11.	What is the use of CIN diplexer?	III	R
12.	What is VSB filter?	III	R
13.	Define AGC.	IV	R
14.	What is use of tuner section?	IV	R
15.	What is Anti hunt network?	IV	R
16.	What is a sync separator?	IV	R

PART-C **(5x10=50 Marks)**

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's level**	**Max marks**
17.	**A.**	Explain monochrome TV transmitter and Receiver with neat block diagram	I	U	10
		(OR)			
	B.	Explain composite video signal (CVS) and CVS for one horizontal line.	I	U	10
18	**A.**	Explain working principle of Vidicon and Plumbicon camera tube.	II	U	10
		(OR)			
	B.	Explain construction and working of monochrome picture tube with neat diagram	II	U	10
19.	**A.**	Explain low level IF modulated TV transmitter with neat block diagram.	III	U	10
		(OR)			
	B.	Explain PAL colour coder with neat block diagram.	III	U	10
20.	**A.**	Explain monochrome receiver with neat block diagram.	IV	U	10
		(OR)			
	B.	Explain high frequency & low frequency compensation.	IV	U	10
21.	**A.**	Explain digital color TV receiver with neat block diagram.	V	U	10
		(OR)			
	B.	Explain telecine equipment with neat block diagram.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 632 TEST ENGINEERING
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's level**
1.	Define Test engineering.	I	R
2.	Define Digital Guarding.	II	R
3.	Mention the Passive and Active Components.	III	U
4.	Expand BSDL.	IV	R
5.	Expand SVF.	IV	U
6.	Define Digital Simulator.	V	R
7.	Mention the characteristics of Passive and Active Components.	III	U
8.	Mention the application of Boundary Scan Test.	IV	U

PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's level**
9.	Define passive and active components.	III	R
10.	Mention need and importance of Test Engineering	I	R
11.	Define auto compensation	II	R
12.	Explain Digital Integrated Circuits.	II	U
13.	Define Clock Termination.	II	R
14.	Mention the need of boundary scan Test technique.	IV	R
15.	Explain JTAG Port.	IV	U
16.	Explain Test Fixtures.	V	U

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's level**	**Max marks**
17.	**A.**	Explain the principles of fundamental Testing Methods and Memory Testing.	I	U	10
		(OR)			
	B.	Explain Manual and Automated PCB Trouble Shooting Techniques.	I	U	10
18	**A.**	Explain functional Testing of Digital, Analog and Mixed Integrated Circuit.	II	U	10
		(OR)			
	B.	Explain different types of Memory Module functional Test.	II	U	10
19.	**A.**	Explain Component Identification of Ageing Effects with VI Curve Trace.	III	U	10
		(OR)			
	B.	Explain Input and Output Characteristics of Digital Integrated Circuits.	III	U	10
20.	**A.**	Explain Principle of Boundary Scan Test and Boundary Scan Architecture with neat diagram.	IV	U	10
		(OR)			
	B.	Explain Digital Integrated Circuit Test using Boundary Scan Techniques.	IV	AP	10
21.	**A.**	Explain ATE in PCB Test.	V	AP	10
		(OR)			
	B.	Explain Standard Test Data Format.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 633 MOBILE COMMUNICATION

TEACHING AND SCHEME OFEXAMINATION:

Number of Weeks/ Semester : 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/ Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Mobile communication	5	75	25	75	100	3 Hrs

TOPICS AND ALLOCATION:

UNIT	TOPIC	TIME (Hrs)
I	Introduction to Mobile Communication	13
II	Broadcast Systems	13
III	Wireless Transmission (2G)	13
IV	Wireless Networking (3G)	12
V	Mobile Network Layer & Transport Layer	12
Revision Test		12
TOTAL		**75**

Course description:

Communication is one of the integral parts of science that has always been a focus point for exchanging information among parties at locations physically apart. After its discovery, telephones have replaced the telegrams and letters. Similarly, the term ‘mobile’ has completely revolutionized the communication by opening up innovative applications that are limited to one’s imagination. Today, mobile communication has become the backbone of the society. All the mobile system technologies have improved the way of living. It’s main plus point is that it has privileged a common mass of society. In this subject, the evolution as well as the fundamental techniques of the mobile communication is discussed.

OBJECTIVES:

- To know the basics of Mobile Radio communication
- To know about wireless communications systems
- To understand the Cellular concept
- To study broadcasting
- To learn the Digital audio and video broadcasting
- To learn the convergence of mobile communications
- To know wireless communications and the process of transmission
- To study about various architectures in wireless transmission
- To study the CDMA digital standards
- To understand Mobile Services (2G), (2.5G) and (3G)
- To know the GPRS and WAP
- To learn the manufacture and operator technologies
- To learn mobile network layer & transport layer
- To study the Dynamic host configuration protocol To know the TCP &its improvements

COURSE OUTCOMES

ECC 633 MOBILE COMMUNICATION	
After successful completion of this course, the students should be able to	
C 633.1	Explain about Mobile communication and cellular concepts.
C 633.2	Explain about broadcasting techniques in mobile communications.
C 633.3	Interpret the concepts of Wireless Transmission (2G).
C 633.4	Show the knowledge on wireless networking (3G).
C 633.5	Interpret about mobile network layer and transport layer.

ECC 633 MOBILE COMMUNICATION

UNITI

INTRODUCTION TO MOBILE COMMUNICATION **[13Hrs]**

Evolution of Mobile Radio Communication, Mobile Radio Telephony in India and around the world [1Hr]

Examples of Wireless Communication Systems: Paging system, [2Hrs]

Cordless telephones systems, Cellular telephone Systems, Trends in Cellular Radio and personal Communications [2Hrs]

THE CELLULAR CONCEPT:

Frequency reuse, Channel Assignment strategies [2Hrs]

Hand off Strategies, Prioritizing Handoffs, Interference and system capacity, [2Hrs]

Improving coverage and capacity in cellular systems ,Cell splitting [2Hrs]

Sectoring, Repeaters for range extension [2Hrs]

UNIT II

BROADCAST SYSTEMS **[13Hrs]**

Introduction – Cyclical repetition of data – [2Hrs]

Digital audio broadcasting – [2Hrs]

multimedia object transfer protocol – [2Hrs]

Digital video broadcasting – [2Hrs]

DVB data broadcasting, [2Hrs]

DVB for high speed internet access – [2Hrs]

Convergence of broadcasting and mobile communications [1Hr]

UNIT III

WIRELESS TRANSMISSION (2G) **[13Hrs]**

Global system for mobile (GSM) - services and features – [2Hrs]

Radio subsystem - channel types - Example of a GSM call – [2Hrs]

Frame structure for GSM – DECT system architecture, [2Hrs]

protocol architecture – TETRA – [1Hr]

UMTS and IMT- 2000 - radio interface, UTRAN, core network, handover – [3Hrs]

CDMA digital cellular standard (IS – 95): Frequency and channel specifications – Forward CDMA channel and Reverse CDMA channel [3Hrs]

UNIT IV

WIRELESS NETWORKING (3G) **[12 Hrs]**

MOBILE SERVICES (2.5G)

GPRS: GPRS Functional groups – architecture - network nodes – [2Hrs]

Procedures - billing [1Hr]

WAP: WAP Model - WAP Gateway- WAP Protocols - WAP UA prof and

caching, wireless bearers for WAP, WAP developer tool kits – Mobile station [1Hr]

application execution environment. [1Hr]

MOBILE SERVICES (3G):

Paradigm Shifts in 3G Systems - W-CDMA and CDMA 2000 – [2Hrs]

Improvements on core network - Quality of service in 3G – [1Hr]

Wireless OS for 3G handset - 3G [1Hr]

systems and field trials - Other trail systems - Impact on manufacture and [2Hrs]

operator technologies [1Hr]

UNIT V

MOBILE NETWORK LAYER & TRANSPORT LAYER **[12 Hrs]**

Mobile IP – Goals, assumptions and requirements, Entities and terminology, [2Hrs]

IP Packet delivery, Agent discovery, Registration, tunneling and encapsulation [2Hrs]

Optimization, Reverse tunneling, IPv6, IP micro- mobility support –

Dynamic host configuration protocol – mobile ad-hoc network – routing [2Hrs]

Destination sequence distance vector – Dynamic source routing –

alternative metrics, TCP – Congestion control – slow start – [2Hrs]

fast retransmit/ fast recovery – implications of mobility – [1Hr]

Classical TCP improvements – indirect – snooping – [1Hr]

Mobile–Transmission timeout freezing – selective retransmission- [2Hrs]

Transaction oriented – TCP over 2.5/3G wireless networks –

Revision and Test **[12 Hrs]**

TEXT BOOKS :

SL.No	Title	Author	Publisher with Edition
1.	Wireless Communications Principles and Practice	Theodore S. Rappaport	Pearson Education, 2003
2.	Mobile Communications	Jochen Schiller	Pearson Education, 2009, Second edition

REFERENCE BOOKS:

SL. No	Title	Author	Publisher with Edition
1.	Wireless and Mobile Network Architectures	Yi-BingLin, Imrich Chlamtac	Wiley, 2001
2.	Mobile Cellular Communication	Gottapu Sasibhushana Rao	Pearson Education, 2012
3.	Wireless Digital Communications	Kamilo Feher	PHI, 2003
4.	Mobile Cellular Communications	W.C.Y. Lee	2nd Edition, MC Graw Hill, 1995
5.	Wireless Networks	P. Nicopolitidis	Wiley, 2003
6.	Wireless Communications and Networks	William Stallings	2nd Edition,Prentice Hall of India-2006

LEARNING WEBSITES

1. https://www.javatpoint.com/mobile-communication-introduction
2. https://electronicsforu.com/technology-trends/mobile-communication-1g-4g
3. https://www.electroschematics.com/5231/mobile-phone-how-it-works/
4. https://www.igi-lobal.com/dictionary/communicame/34130
5. https://www.tutorialspoint.com/umts/umts_history_of_mobile_communication.htm

CONTINUOUS INTERNAL ASSESSMENT

The Internal Assessment marks for a total of 25 marks, which are to be distributed as follows:

i)	Attendance	-	5 Marks
ii)	Test	-	10 Marks
iii)	Assignment	-	5 Marks
iv)	Seminar	-	5 Marks

	Total	**-**	**25 Marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 633.1	3	3	3	3	3	2	3	3	2	3
C 633.2	3	3	3	3	3	2	3	3	2	3
C 633.3	3	3	3	3	3	2	3	3	2	3
C 633.4	3	3	3	3	3	2	3	3	2	3
C 633.5	3	3	3	3	3	2	3	3	2	3
C 633	15	15	15	15	15	10	15	15	10	15
Correlation Level	3	3	3	3	3	2	3	3	2	3

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

QUESTION PAPER SETTING

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Embedded systems practical	4	60	25	75	100	3 Hrs

The teaching leering process and assessment are being carried out in accordance with the revised Bloom's Taxonomy. The question paper should consist of 90% questions based on Lower Order Thinking (LOTs) and the remaining 10% based on Higher Order Thinking (HOTs) as detailed below.

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 640 EMBEDDED SYSTEMS PRACTICAL

TEACHING AND SCHEME OF EXAMINATION:

No of weeks per semester: 15 weeks

ALLOCATION OF MARKS

Title	Marks
Algorithm/flow chart	15
Program	25
Execution	20
Result	10
Viva	5
Total	75

Course description

ARM is a major processor widely used in the embedded system in products ranging from cell/mobile phones to automotive braking and control systems. Since 1985, the ARM architecture has become the most pervasive 32-bit architecture in the world. This practical course has been set up to describe the operation of the ARM core from experimenting simple exercises with a clear emphasis on its architecture by assuming no previous ARM experience. In Diploma level, the ARM architecture is studied and experimented for its internals through hands on. This is achieved by experiencing the experiments through industrial and society describe the system requirement and to make a complete prototype working model.

LIST OF EQUIPMENTS AND REQUIREMENTS:

1. ARM7 TDMI Kit – 10 nos with interface boards for the above experiments The Chip set may be TMS470, LPC2138, LPC2148, or STR7 etc
2. Interfaces:RTC, ADC, LCD, Seven segment display, LEDS and Switches.
3. Manual for the kit and for interfacing board with stepper motor
4. Manual for the built in function for the Board

OBJECTIVES:

On completion of the following exercises, the students must be able to

- To study the Processor kit
- To develop and executed an assembly level program
- To realizing the timer peripheral in ARM by using :polling and interrupt driven method
- To develop and realize the ASM
- To access the programs by using LCD in ARM processor
- To interface stepper motor in ARM processor
- To implement, creating and Deleting the task by using RTOS.

COURSE OUTCOMES

ECC 640 EMBEDDED SYSTEMS PRATICAL	
After successful completion of this course, the students should be able to	
C 640.1	Explain about ARM processor kit and simulate arithmetic operation, soft delay and LED blinking with variable speed.
C 640.2	Develop the input and output port in ARM **,**timer peripheral in ARM by polling method and timer peripheral in ARM by interrupt driven method.
C 640.3	Develop C Program and execute serial transmission and reception of a character by interrupt method, displaying alphanumeric characters in 2x16 line LCD module.
C 640.4	Develop the program for converting hexadecimal to decimal and to display in LCD.
C 640.5	Elaborate the Interfacing the stepper motor in ARM processor and generation of PWM

ECC 640 EMBEDDED SYSTEMS PRACTICAL

S.No	Name of the experiment	Course Outcome
1	**STUDY OF ARM PROCESSOR KIT** (whatever the ARM processor kit the institution is having) Example: LPC2148 The student should able to Understand the memory mapping of the IO and peripherals List the peripherals present in the processor Explain that how to use an IO pin, related SFRs and instructions Explain that how to use timer, UART, its related SFR and instructions sets	**C 640.1**
2	**SIMULATION OF ARITHMETIC OPERATION ON ARM IN ASSEMBLY** Develop an assembly level code for the single precision (32 bit) arithmetic function. a. Addition, b. Subtraction and b. Multiplication (Note: simulate the program in the software)	**C 640.1**
3	**SIMULATION OF ASSEMBLY LEVEL PROGRAM FOR SOFT DELAY** Develop an assembly level code for the 32 bit or 64 bit delay routine. Calculate the no of clock taken for the routine and adjust the delay value for the desired. (Note: simulate the program in the software)	**C 640.1**
4	**SIMPLE LED BLINKING WITH VARIABLE SPEED IN ASM** Develop an assembly level program of ARM processor to blink a LED (including delay routine) in variable speed in the trainer kit. Upon change in the delay program the speed should vary. No need to change the speed dynamically. (Note: Student should study the list of special function registers associated for accessing the IO pin. Manual containing List of IO registers (SFR for IO) can be given to the students for the final exam)	**C 640.1**
5	**REALIZATION OF INPUT AND OUTPUT PORT IN ASM** Develop an assembly level program of ARM processor to read a port in which switches are connected in the trainer kit. Send back the receive input to output in which LEDs are connected in the trainer kit Note: Student should study the list of special function registers associated for accessing Port the read and write. Manual containing List of IO registers (SFR for IO) can be given to the students for the board exam)	**C 640.2**
6	**SIMPLE LED BLINKING WITH VARIABLE SPEED IN C** Develop a C program for ARM processor to blink a LED (including delay routine) in variable speed. Upon change in the input switch the speed should vary. (Note: The C code should be in while loop)	**C 640.2**
7	**SEVEN SEGMENT LED DISPLAY INTERFACE IN C** Develop a C program for ARM processor to interface a seven segment LED display. The display should count up for every one second.	**C 640.2**
8	**SEVEN SEGMENT LED DISPLAY INTERFACE IN C** Develop a C program for ARM processor to interface a seven segment LED display. The display should count up for every one second. The delay can be used from experiment.	**C 640.2**
9	**REALIZING TIMER PERIPHERAL IN ARM BY POLLINGMETHOD** Develop a C program for ARM processor to run a timer peripheral in ARM. The timer flag can be pooled for timer end. As timer ends reset the timer and update new value to the LED display.	**C 640.1**

10	**REALIZING TIMER PERIPHERAL IN ARM BY INTERRUPT DRIVEN METHOD** Develop a C program for ARM processor to run a timer peripheral in ARM. The timer flag can be pooled for timer end. As timer ends reset the timer and update new value to the LED display.	**C 640.2**
11	**SERIAL TRANSMISSION AND RECEPTION OF A CHARACTER IN C BY POLLING METHOD** Write a C Programs for receiving a character from other device (Computer) and send the next character of the received one to the device back. Note: Student should understand the SFRs used for serial communication. Manual containing list of SFRs for the UART can be given to the students for their final examination	**C 640.2**
12	**SERIAL TRANSMISSION AND RECEPTION OF A CHARACTER IN C BY INTERRUPT METHOD** Write a C Programs for receiving a character from other device (Computer) and send the next character of the received one to the device back.	**C 640.3**
13	**DISPLAYING ALPHANUMERIC CHARACTERS IN 2X16 LINE LCD MODULE** Write a C Programs for displaying a number and an alphabet in the LCD module by just calling the built in LCD function. The display should come in the desired line and column. (Built in function for the LCD can be given in the manual)	**C 640.3**
14	**CONVERTING HEXADECIMAL TO DECIMAL AND TO DISPLAY IN LCD** Write a C Programs for converting the given 8 bit hexadecimal into decimal and there by converting into ASCII which is to be displayed in the LCD module. (Built in function for the LCD can be given in the manual)	**C 640.4**
15	**ACCESSING INTERNAL ADC OF THE ARM PROCESSOR AND TO DISPLAY IN LCD** Write a C Program for reading an ADC, convert into decimal and to display it The ADC input is connected to any analog sensor. (Note: Student should study the SFR associated with ADC, Manual containing List of SFR for accessing ADC can be given for the examination.)	**C 640.4**
16	**ACCESSING INTERNAL ADC OF THE ARM PROCESSOR AND TO DISPLAY IN LCD** Write a C Program for reading an ADC, convert into decimal and to display it The ADC input is connected to any analog sensor. (Note: Student should study the SFR associated with ADC, Manual containing List of SFR for accessing ADC can be given for the examination.)	**C 640.4**
17	**INTERFACING STEPPER MOTOR IN ARM PROCESSOR** Write a C programs for running stepper motor either in clock wise or counter clock wise.A switch used for selecting the direction of the rotation. (Note: students should study the SFR associated with RTC, Manual containing list of SFR for accessing RTC can be given for the examination)	**C 640.5**
18	**GENERATION OF PWM** Write C program to generate a PWM signal	**C 640.5**

Learning websites

https://www.slideshare.net/nirajbharambe/embedded-system-practical-manual-1

https://muresults.net/itacademic/Workshopdata/ES.pdf

http://www.inf.ed.ac.uk/teaching/courses/es/PDFs/Coursework-2.pdf

http://www.inf.ed.ac.u

https://www.researchgate.net/publication/272485567_Practical_Aspects_of_Embedded_System_Design_using_Microcontrollersk/teaching/courses/es/PDFs/Coursework-2.pdf

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

s) Attendance : 5 marks – (Award of marks same as theory subjects)

t) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

u) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C 640.1	3	3	3	3	3	3	3	2	3	3
C 640.2	3	3	3	3	3	3	3	2	3	3
C 640.3	3	3	3	3	3	3	3	2	3	3
C 640.4	3	3	3	3	3	3	3	2	3	3
C 640.5	3	3	3	3	3	3	3	2	3	3
C 640	15	15	15	15	15	15	15	10	15	15
Correlation Level	3	3	3	3	3	3	3	2	3	3

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

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ECC 650 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester: 15 weeks

Course	Instruction		Examination			
	Hrs/ Week	Hrs / Semester	Marks			Duration
			Internal Assessment	Semester End Examination	Total	
Computer Hardware Servicing and Networking Practical	4	60	25	75	100	3 Hrs

ALLOCATION OF MARKS:

CONTENT	MAX. MARKS	
	PART - A	PART - B
Procedure	15	15
Execution	15	15
Result with printout	5	5
Viva	5	
Total	75	

Course Description

The course aims at making the students familiar with various parts of computers and laptops and how to assemble them and the different types of peripherals desired. In addition, the course will provide the students with necessary knowledge and skills in computer and laptop software installation and maintenance and to make him diagnose the software faults. This subject also gives the knowledge and competency to diagnose systematic repair and maintenance of computers and laptops

HARDWARE REQUIREMENTS :

Computer with Pentium / Core processors with inbuilt NIC -30 Nos

Hard disk drive -02 Nos

CDD/ DVD Writer -02 Nos

Blank Blu-ray disk -30 Nos

Web camera -02 Nos

Laser Printer -02 Nos

Dot matrix Printer -02 Nos

Blank DVD -30 Nos

Scanner -02 Nos

Laptop -02 Nos

Bio metric device -02 Nos

Crimping Tool -06 Nos

Network Cables

RJ45 Tester -06 Nos

Modem with internet connection -02 Nos

Hub -02 Nos

Switch/ Router -02 Nos

SOFTWARE REQUIREMENTS:

Windows XP operating system/ Windows 7 OS

DVD/ CD Burning S/W (Ahead Nero or latest S/W)

OBJECTIVES

- On completion of the following exercises, the students must be able to
- Know the various indicators, switches and connectors used in Computers.
- Familiarize the layout of SMPS, motherboard and various Disk Drives.
- Configure Bios set up options.
- Install various secondary storage devices with memory partition and formatting.
- Know the various types of printer installation and to handle the troubleshooting ability.
- Acquire the practical knowledge about the installation of various devices like scanner, web camera, cell phone and bio-metric devices.
- Assemble PC system and checking the working condition.

COURSE OUTCOMES

ECC 650 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL	
After successful completion of this course, the students should be able to	
C650.1	Identify the system layout, installation of hard disk and DVD/BLU-ray writer
C650.2	Explain the Installation and configuring printer, Scanner , Web cam and bio-metric device
C650.3	Demonstrate the Installation OS and Dual OS in the assembled system and assemble and disassemble a Laptop to identify the parts and install OS in the laptop.
C650.4	Demonstrate the Cabling works for establishing a network ,Crimp the network cable with RJ 45 connector and test the crimped cable using a cable tester and interface two PCs to form Peer To Peer network using the connectivity devices Switch or Router in a LAN .
C650.5	Interpret the Sharing of the files,folders, printer in a LAN, Configure DNS, Install and configure Network Devices: HUB,Switch or Routers, Install and configure a DHCP server and Connect the computer in local area network.

ECC 650 COMPUTER HARDWARE SERVICING AND NETWORKING PRACTICAL

S. No	Name of the experiment	Course Outcome
1	**PART A – COMPUTER HARDWARE SERVICING** **IDENTIFICATION OF SYSTEM LAYOUT** i) Identify front panel indicators & switches and Front side & rear side connectors ii) Familiarize the computer system layout by marking positions of SMPS, Motherboard, FDD, HDD, CD, DVD and add on cards.	**C650.1**
2	**HARD DISK** i) Configure bios setup program and troubleshoot the typical problems using BIOS utility. ii) Install, Configure, Partition and Format Hard disk.	**C650.1**
3	**DVD/BLU-RAY WRITER** i) Install and Configure a DVD Writer and record a blank DVD. ii) Install and Configure a Blu-ray Writer and record a blank Blu-ray Disc.	**C650.1**
4	**Printer Installation** i) Install and configure Dot matrix printer ii) Install and configure Laser printer	**C650.2**
5	i) Install and configure Scanner ii) Install and configure Web cam and bio-metric device	**C650.2**
6	i) Assemble a system with add on cards and check the working condition of the system ii) Install OS in the assembled system.	**C650.3**
7	Install Dual OS in a system	**C650.3**
8	i) Assemble and Disassemble a Laptop to identify the parts. ii) Install OS in the laptop.	**C650.3**
9	**PART B – COMPUTER NETWORKING** Do the following Cabling works for establishing a network i) Crimp the network cable with RJ 45 connector in Standard cabling mode and cross cabling mode. ii) Test the crimped cable using a cable tester.	**C650.4**
10	Use IPCONFIG, PING , TRACERT and NETSTAT utilities to debug the network issues.	**C650.4**
11	Interface two PCs to form Peer To Peer network using the connectivity devices Switch or Router in a LAN .	**C650.4**
12	Share the files and folders in a LAN.	**C650.5**
13	Share a printer in a LAN.	**C650.5**
14	Configure DNS to establish interconnection between systems and describe how a name is mapped to IP Address	**C650.5**
15	i) Install and configure Network Devices: HUB, Switch or Routers ii) Install and Configure NIC.	**C650.5**
16	Install and configure a DHCP server in windows with IP address ranging from 192.168.1.1 to 192.168.1.100 and configure a DHCP client	**C650.5**
17	Connect the computer in local area network.	**C650.5**

Learning websites

https://www.academia.edu/22093398/COMPUTER_HARDWARE_SERVICING_ICT-COMPUTER_HARDWARE_SERVICING

http://chs-comtipz.blogspot.com/2015/01/terms-for-computer-hardware-servicing.html

https://www.finduniversity.ph/majors/computer-hardware-servicing-2-philippines/

https://www.nvtighana.org/pdf/SYLLABUS/COMPUTER%20HARDWARE.pdf

http://tesda3.com.ph/-downloads/TR-Computer-Hardware-Servicing-NC-II.doc

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

d) Attendance : 5 marks – (Award of marks same as theory subjects)

e) Procedure/ observation and tabulation/ Other Practical related work : 10 marks

f) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C650.1	3	3	3	3	3	3	3	2	2	3
C650.2	3	3	3	3	3	3	3	2	2	3
C650.3	3	3	3	3	3	3	3	2	2	3
C650.4	3	3	3	3	3	3	3	2	2	3
C650.5	3	3	3	3	3	3	3	2	2	3
C650	15	15	15	15	15	15	15	10	10	15
Correlation level	3	3	3	3	3	3	3	2	2	3

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

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ECC 660 ADVANCED MICROCONTROLLER AND SIMULATION PRACTICAL

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester : 15 weeks

Course	Instruction		Examination			
			Marks			Duration
	Hrs/Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	
Simulation Practical	4	60	25	75	100	3 Hrs

ALLOCATION OF MARKS

I) Program / Circuit Design	– 25 Marks
II) Execution	– 25 Marks
III) Result	– 20 Marks
IV) Viva – Voice	– 5 Marks
TOTAL	**75 Marks**

Course Description

To design and verify the results of various electronic circuits using simulation software and verify the result in the computer. Today engineering field has developed to a great extent that there is always the need for study of various simulation concepts for doing the experiments instead of doing the experiments in laboratory. This lab is fulfill the need for students to study the simulation software and able to design the various Electronic circuits like Rectifier circuits, Waveform Generator, Single side & Multilayer PCB layout.

OBJECTIVES

At the end of the course , the students will be able to,

- Design the Rectifier circuits like Half wave, Full wave & Bridge rectifiers with filters.
- Design a Power Supply with Regulators.

- Construct the Waveform Generator using transistors
- Design the circuits for Clipper & Clamper, Op-am applications, Instrumentation amplifiers.
- Design the Modulation & Demodulation circuits like AM,FM, ASK,FSK,PSK.
- Design the Single side & Multilayer PCB layout using CAD tool
- Design the ATMEGA2560 advanced microcontroller Kit with simple programmes.

COURSE OUTCOMES

ECC 660 ADVANCED MICROCONTROLLER AND SIMULATION PRACTICAL	
After successful completion of this course, the students should be able to	
C660.1	Explain about ATMEGA2560 advanced microcontroller Kit **.**
C660.2	Develop and implement the program for moving the robot , white line follower, obstacle avoidance with buzzer indication,2x16 LCD interface for welcome display
C660.3	Design the Simulating circuits of Rectifier circuits (Half wave, Full wave & Bridge rectifiers with filters) Astable multivibrators and monostable multivibrators .
C660.4	Design the Simulating circuits of the Clippers & Clampers, Op-amp Application, Instrumentation amplifiers
C660.5	Design the Simulating circuits of the AM , FM, ASK ,FSK , PSK Modulation and Demodulation circuits.

ECC 660 ADVANCED MICROCONTROLLER AND SIMULATION PRACTICAL

S.No	Name of the experiment	Course Outcome
1	Study of ATMEGA2560 advanced microcontroller Kit	C660.1
2	Develop and implement the program for moving the robot in forward and backward direction using ATMEGA2560 microcontroller	C660.2
3	Develop the program for white line follower robot using ATMEGA2560 microcontroller.	C660.2
4	Develop the program for obstacle avoidance with buzzer indication using ATMEGA2560 microcontroller.	C660.2
5	Develop the program for obstacle avoidance with buzzer indication using ATMEGA2560 microcontroller.	C660.2
6	Develop the program for 2x16 LCD interface for welcome display using ATMEGA2560 microcontroller.	C660.2
7	SIMULATION PRACTICAL Note : All experiments should be designed and verified through SPICE simulation tool (like PSPICE/Multisim/Lab VIEW/OrCAD/TINA) Rectifier circuits (Half wave, Full wave & Bridge rectifiers with filters)	C660.3
8	Power supply design with regulators (Astable multivibrators)	C660.3
9	Waveform generators using transistors (Astable multivibrators)	C660.3
10	Waveform generators using transistors (monostable multivibrators)	C660.3
11	Clippers & Clampers.	C660.4
12	Op-amp Application – I (any three circuits) (Inverting and non-inverting amplifiers, Voltage follower, Integrator, Differentiator, Summing amplifier, Difference amplifier)	C660.4
13	Instrumentation amplifiers	C660.4
14	AM Modulation and Demodulation	C660.5
15	FM Modulation and Demodulation	C660.5
16	ASK Modulation and Demodulation	C660.5
17	FSK Modulation and Demodulation	C660.5
18	PSK Modulation and Demodulation	C660.5

Learning websites

1.https://www.mhlnews.com/technology-amp-automation/practical-sim 2.https://e

https://www.josoorinstitute.qa/education-3.development/courses/Practical-

4.Simulationn.wikipedia.org/wiki/Computer_simulationulation

5.https://www.sciencedirect.com/science/article/pii/S0734242X83710153

Continuous Internal Assessment

The Internal Assessment mark for a total of 25 marks which are to be distributed as follows:-

d) Attendance : 5 marks – (Award of marks same as theory subjects)

e) Procedure/ observation and tabulation/

Other Practical related work : 10 marks

f) Record writing : 10 marks

Total **25 marks**

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C660.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C660	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

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ECC 670 PROJECT WORK

TEACHING AND SCHEME OF EXAMINATION

No. of weeks per semester : 15 weeks

course	Instruction		Examination			
			Marks			
	Hrs/Week	Hrs / Semester	Internal Assessment	Semester End Examination	Total	Duration
Project Work	5	75	25	75	100	3 Hrs

OBJECTIVES:

- The project is aimed to assemble test a photo type model of any one item/gadget
- Real time application problems if any may be identified from any industry and maybe chosen
- The knowledge and the skill so far acquired may be made use of.
- The team spirit may be motivated
- The entrepreneurship ideas may be motivated by conducting a career guidance programme
- Learn and understand the gap between the technological knowledge acquired through curriculam and the actual industrial need and to compense it by acquiring additional knowledge as required.

Detail of Assessment	Period of Assessment	Max. Marks
First Review	6 th week	10
Second Review	15 th week	10
Attendance	Entire semester	5
Total		25

COURSE OUTCOMES

ECC 670 PROJECT WORK	
After successful completion of this course, the students should be able to	
C670.1	Identify Real time application problems and apply the acquired knowledge and skills to solve it.
C670.2	Design ,assemble and test a proto type model.
C670.3	Show the team spirit and get motivated.
C670.4	Develop the entrepreneurship ideas through career guidance programme
C670.5	Analyze the gap between the technological knowledge acquired through curriculum and the actual industrial needs and to compensate it by acquiring additional knowledge as required.

EVALUATION FOR AUTONOMOUS EXAMINATION:

PROJECT WORK

The Students of all the Diploma courses have to do a Project Work as part of the Curriculum and in Partial fulfillment for the award of Diploma by the State Board of Technical Education and Training, Tamil Nadu. In order to encourage students to do worthwhile and innovative projects, every year prizes are awarded for the best three projects i.e. institution wise, region wise and state wise. **The Project work must be reviewed twice in the same semester.**

e) Internal Assessment Mark for Project Work & Viva Voce

Project Review I	:	10 Marks
Project Review II	:	10 marks
Attendance	:	05 marks (Award of marks same as theory subject pattern)
Total	**:**	**25 marks**

Proper record to be maintained for the two project reviews, and it should be preserved for 2 semesters and produced to the flying squad and the inspection team at the time of inspection/ verification.

Allocation of Marks for project work & Viva Voce in Autonomous Examination

Viva Voce	:	30 marks
Marks for Report Preparation & Demo	:	35 marks
Total	**:**	**65 marks**

f) Written Test Mark (from 2 topics for 30 minutes duration) #

v)	Environment Management	2 questions x 2 ½ marks	= 5 marks
vi)	Disaster Management	2 questions x 2 ½ marks	= 5 marks
			10 marks

Selection of questions should be from Question Bank, by the External Examiner, No Choice need be given to the candidates

Project Work & Viva Voce in Autonomous Examination	- 65 Marks
Written Test Mark (from 2 topics for 30 minutes duration)	- 10 Marks
Total	**75 marks**

A neatly prepared PROJECT REPORT as per the format has to be submitted by individual student during the project Work & Viva voce Autonomous Examination.

DETAILED SYLLABUS

ENVIRONMENTAL & DISASTER MANAGEMENT

1. ENVIRONMENTAL MANAGEMENT Introduction – Environmental Ethics – Assessment of Socio Economic Impact – Environmental Audit – Mitigation of adverse impact on Environment – Importance of Pollution Control – Types of Industries and Industrial Pollution.

Solid waste management – Characteristics of Industrial wastes – Methods of Collection, transfer and disposal of solid wastes – Converting waste to energy – Hazardous waste management Treatment technologies.

Waste water management – Characteristics of Industrial effluents – Treatment and disposal methods – Pollution of water sources and effects on human health.

Air pollution management – Sources and effects – Dispersion of air pollutants – Air pollution control methods – Air quality management.

Noise pollution management – Effects of noise on people – Noise control methods.

2. DISASTER MANAGEMENT Introduction – Disasters due to natural calamities such as Earthquake, Rain, Flood, Hurricane, Cyclones etc – Man made Disasters – Crisis due to fires, accidents, strikes etc – Loss of property and life..
Disaster Mitigation measures – Causes for major disasters – Risk Identification – Hazard Zones – Selection of sites for Industries and residential buildings – Minimum distances from Sea – Orientation of Buildings – Stability of Structures – Fire escapes in buildings - Cyclone shelters – Warning systems.

Disaster Management – Preparedness, Response, Recovery – Arrangements to be made in the industries / factories and buildings – Mobilization of Emergency Services - Search and Rescue operations – First Aids – Transportation of affected people – Hospital facilities – Fire fighting arrangements – Communication systems – Restoration of Power supply – Getting assistance of neighbors / Other organizations in Recovery and Rebuilding works – Financial commitments – Compensations to be paid – Insurances – Rehabilitation.

LIST OF QUESTIONS

1. ENVIRONMENTRAL MANAGEMENT

1. What is the responsibility of an Engineer-in-charge of an Industry with respect to Public Health?
2. Define Environmental Ethic.
3. How Industries play their role in polluting the environment?
4. What is the necessity of pollution control? What are all the different organizations you know, which deal with pollution control?
5. List out the different types of pollutions caused by a Chemical / Textile / Leather / Automobile / Cement factory.
6. What is meant by Hazardous waste?
7. Define Industrial waste management.
8. Differentiate between garbage, rubbish, refuse and trash based on their composition and source.
9. Explain briefly how the quantity of solid waste generated in an industry could be reduced.
10. What are the objectives of treatments of solid wastes before disposal?
11. What are the different methods of disposal of solid wastes?
12. Explain how the principle of recycling could be applied in the process of waste minimization.
13. Define the term 'Environmental Waste Audit'.
14. List and discuss the factors pertinent to the selection of landfill site.
15. Explain the purpose of daily cover in a sanitary landfill and state the minimum desirable depth of daily cover.
16. Describe any two methods of converting waste into energy.
17. What actions, a local body such as a municipality could take when the agency appointed for collecting and disposing the solid wastes fails to do the work continuously for number of days?
18. Write a note on Characteristics of hazardous waste.
19. What is the difference between municipal and industrial effluent ?
20. List few of the undesirable parameters / pollutants anticipated in the effluents from oil refinery industry / thermal power plants / textile industries / woolen mills / dye industries / electroplating industries / cement plants / leather industries (any two may be asked)
21. Explain briefly the process of Equalization and Neutralization of waste water of varying characteristics discharged from an Industry.
22. Explain briefly the Physical treatments "Sedimentation" and "Floatation" processes in the waste water treatment.
23. Explain briefly when and how chemical / biological treatments are given to the waste water.
24. List the four common advanced waste water treatment processes and the pollutants they remove.
25. Describe refractory organics and the method used to remove them from the effluent.
26. Explain biological nitrification and de-nitrification.
27. Describe the basic approaches to land treatment of Industrial Effluent.
28. Describe the locations for the ultimate disposal of sludge and the treatment steps needed prior to ultimate disposal.
29. List any five Industries, which act as the major sources for Hazardous Air Pollutants.

30. List out the names of any three hazardous air pollutants and their effects on human health.
31. Explain the influence of moisture, temperature and sunlight on the severity of air pollution effects on materials.
32. Differentiate between acute and chronic health effects from Air pollution.
33. Define the term Acid rain and explain how it occurs.
34. Discuss briefly the causes for global warming and its consequences
35. Suggest suitable Air pollution control devices for a few pollutants and sources.
36. Explain how evaporative emissions and exhaust emissions are commonly controlled.
37. What are the harmful elements present in the automobile smokes? How their presence could be controlled?
38. What is the Advantage of Ozone layer in the atmosphere? State few reasons for its destruction.
39. Explain the mechanism by which hearing damage occurs.
40. List any five effects of noise other than hearing damage.
41. Explain why impulsive noise is more dangerous than steady state noise.
42. Explain briefly the Source – Path – Receiver concept of Noise control.
43. Where silencers or mufflers are used ? Explain how they reduce the noise.
44. Describe two techniques to protect the receiver from hearing loss when design / redress for noise control fail.
45. What are the problems faced by the people residing along the side of a railway track and near to an Airport? What provisions could be made in their houses to reduce the problem?

2. DISASTER MANAGEMENT

1. What is meant by Disaster Management? What are the different stages of Disaster management?
2. Differentiate Natural Disasters and Man made Disasters with examples.
3. Describe the necessity of Risk identification and Assessment Surveys while planning a project.
4. What is Disasters recovery and what does it mean to an Industry?
5. What are the factors to be considered while planning the rebuilding works after a major disaster due to flood / cyclone / earthquake? (Any one may be asked)
6. List out the public emergency services available in the state, which could be approached for help during a natural disaster.
7. Specify the role played by an Engineer in the process of Disaster management.
8. What is the cause for Earthquakes? How they are measured? Which parts of India are more vulnerable for frequent earthquakes?
9. What was the cause for the Tsunami 2004 which inflicted heavy loss to life and property along the coast of Tamilnadu ? Specify its epicenter and magnitude.
10. Specify the Earthquake Hazard Zones in which the following towns of Tamilnadu lie: (a) Chennai (b) Nagapattinam (c) Coimbatore (d) Madurai (e) Salem.
11. Which parts of India are experiencing frequent natural calamities such as (a) heavy rain fall (b) huge losses due to floods (c) severe cyclones
12. Define basic wind speed. What will be the peak wind speed in (a) Very high damage risk zone – A, (b) High damage risk zone, (c) Low damage risk zone.
13. Specify the minimum distance from the Sea shore and minimum height above the mean sea level, desirable for the location of buildings.

14. Explain how the topography of the site plays a role in the disasters caused by floods and cyclones.
15. Explain how the shape and orientation of buildings could reduce the damages due to cyclones.
16. What is a cyclone shelter ? When and where it is provided ? What are its requirements ?
17. What Precautionary measures have to be taken by the authorities before opening a dam for discharging the excess water into a canal/river ?
18. What are the causes for fire accidents ? Specify the remedial measures to be taken in buildings to avoid fire accidents.
19. What is a fire escape in multistoried buildings ? What are its requirements ?
20. How the imamates of a multistory building are to be evacuted in the event of a fire/Chemical spill/Toxic Air Situation/ Terrorist attack, (any one may be asked).
21. Describe different fire fighting arrangements to be provided in an Industry.
22. Explain the necessity of disaster warning systems in Industries.
23. Explain how rescue operations have to be carried out in the case of collapse of buildings due to earthquake / blast / Cyclone / flood.
24. What are the necessary steps to be taken to avoid dangerous epidemics after a flood disaster?
25. What relief works that have to be carried out to save the lives of workers when the factory area is suddenly affected by a dangerous gas leak / sudden flooding ?
26. What are the difficulties faced by an Industry when there is a sudden power failure? How such a situation could be managed?
27. What are the difficulties faced by the Management when there is a group clash between the workers? How such a situation could be managed?
28. What will be the problems faced by the management of an Industry when a worker dies because of the failure of a mechanical device due to poor maintenance? How to manage such a situation ?
29. What precautionary measures have to be taken to avoid accidents to labourers in the Industry in a workshop / during handling of dangerous Chemicals / during construction of buildings / during the building maintenance works.
30. Explain the necessity of medical care facilities in an Industry / Project site.
31. Explain the necessity of proper training to the employees of Industries dealing with hazardous products, to act during disasters.
32. What type of disaster is expected in coal mines, cotton mills, Oil refineries, ship yards and gas plants?
33. What is meant by Emergency Plan Rehearsal? What are the advantages of such Rehearsals?
34. What action you will take when your employees could not reach the factory site because of continuous strike by Public Transport workers?
35. What immediate actions you will initiate when the quarters of your factory workers are suddenly flooded due to the breach in a nearly lake / dam, during heavy rain?
36. What steps you will take to avoid a break down when the workers union of your Industry have given a strike notice?
37. List out few possible crisis in an organization caused by its workers? What could be the part of the middle level officials in managing such crisis?
38. What types of warning systems are available to alert the people in the case of predicted disasters, such as floods, cyclone etc.
39. Explain the necessity of Team work in the crisis management in an Industry / Local body.

40. What factors are to be considered while fixing compensation to the workers in the case of severe accidents causing disability / death to them?
41. Explain the legal / financial problems the management has to face if safely measures taken by them are found to be in adequate.
42. Describe the importance of insurance to men and machinery of an Industry dealing with dangerous jobs.
43. What precautions have to be taken while storing explosives in a match/ fire crackers factory?
44. What are the arrangements required for emergency rescue works in the case of Atomic Power Plants?
45. Why residential quarters are not constructed nearer to Atomic Power Plants?

CO- POs & PSOs MAPPING MATRIX

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PSO1	PSO2	PSO3
C670.1	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670.2	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670.3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670.4	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670.5	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
C670	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**	**15**
Correlation Level	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**

Correlation level 1 – Slight (low)
Correlation level 2 – Moderate (Medium)
Correlation level 3 – Substantial (high)

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ECC 610 EMBEDDED SYSTEMS
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
17.	What is the function of interrupt controller?	II	U
18.	Define endianness.	I	R
19.	What is the use of data processing instructions?	II	U
20.	Explain stack and stack pointer.	II	R
21.	What is cache hit & cache miss?	III	U
22.	What is wake up timer?	IV	R
23.	Define multitasking.	V	R
24.	Define context switching.	V	R

PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
25.	Compare RISC and CISC.	I	An
26.	Write ALP for multiplication.	II	U
27.	Write about data processing instructions supported by ARM.	II	U
28.	Draw the cache architecture and explain.	III	R
29.	Explain UART in detail.	IV	U
30.	Explain flushing of a ARM cache core.	III	U
31.	Explain SLOS in detail.	V	U
32.	What is the purpose of I^2C Interface?	IV	R

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's level**	**Max marks**
17.	**A.**	Explain embedded hardware with neat diagram.	I	U	10
		(OR)			
	B.	Explain ARM design philosophy and development tools.	I	U	10
18	**A.**	Explain Memory management unit with neat block diagram.	II	U	10
		(OR)			
	B.	Explain Cache architecture and cache policies.	II	U	10
19.	**A.**	Explain thump instruction set and load – store instruction set.	III	R	10
		(OR)			
	B.	Explain Interrupts, and IRQ / FIQ exceptions interrupt.	III	R	10
20.	**A.**	Explain Universal Asynchronous Receiver/Transmitter.	IV	U	10
		(OR)			
	B.	Explain General Purpose Input/Output.	IV	U	10
21.	**A.**	Explain Simple Little Operating System.	V	U	10
		(OR)			
	B.	Explain Real-time operating systems.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 620 COMPUTER HARDWARE SERVICING AND NETWORKING
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
17.	What is a Chipset?	I	U
18.	Define: BUS.	I	R
19.	What is the use of ultra ATA?	I	U
20.	What is Blue ray?	I	U
21.	Expand the term LED.	II	R
22.	What is parallel port?	II	R
23.	Expand the term UPS.	II	R
24.	List out the types of printers.	II	U
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
25.	Define: BIOS.	III	R
26.	List out the types of adapter.	III	R
27.	Give the types of RAM.	I	R
28.	Expand POST	III	R
29.	What is half duplex?	IV	U
30.	Give any two advantages of star topology.	IV	U
31.	Expand the term MAN.	IV	R
32.	What are the types of transmission media?	IV	R

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's level**	**Max marks**
17.	**A.**	Explain architecture and block diagram of multicore Processor.	I	U	10
		(OR)			
	B.	Explain hard disk construction and working principle with neat diagram.	I	U	10
18	**A.**	Explain working principle of modem with neat diagram.	II	U	10
		(OR)			
	B.	Explain working principle of SMPS with neat diagram.	II	U	10
19.	**A.**	Explain block diagram of laptop motherboard with neat diagram.	III	AP	10
		(OR)			
	B.	Explain Formatting, Partitioning and Installation of OS.	III	U	10
20.	**A.**	Explain different types of network with neat diagram.	IV	U	10
		(OR)			
	B.	Explain different types of topology with neat diagram.	IV	AP	10
21.	**A.**	Explain Dotted Decimal Notation, Subnetting & Supernetting.	V	An	10
		(OR)			
	B.	Explain TCP/IP protocol.	V	An	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 631 TELEVISION ENGINEERING
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
17.	What is scanning?	I	R
18.	What is meant by flicker?	I	R
19.	Mention any two TV standards	I	R
20.	What is the need for synchronizing pulses?	I	R
21.	Mention the types of camera tube	II	R
22.	What is automatic degaussing?	II	R
23.	Define screen burn	II	R
24.	What is meant by dark current?	II	R
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom'slevel**
25.	What is high level modulation?	III	R
26.	What is the use of visual exciter?	III	R
27.	What is the use of CIN diplexer?	III	R
28.	What is VSB filter?	III	R
29.	Define AGC.	IV	R
30.	What is use of tuner section?	IV	R
31.	What is Anti hunt network?	IV	R
32.	What is a sync separator?	IV	R

PART-C **(5x10=50 Marks)**

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's level**	**Max marks**
17.	**A.**	Explain monochrome TV transmitter and Receiver with neat block diagram	I	U	10
		(OR)			
	B.	Explain composite video signal (CVS) and CVS for one horizontal line.	I	U	10
18	**A.**	Explain working principle of Vidicon and Plumbicon camera tube.	II	U	10
		(OR)			
	B.	Explain construction and working of monochrome picture tube with neat diagram	II	U	10
19.	**A.**	Explain low level IF modulated TV transmitter with neat block diagram.	III	U	10
		(OR)			
	B.	Explain PAL colour coder with neat block diagram.	III	U	10
20.	**A.**	Explain monochrome receiver with neat block diagram.	IV	U	10
		(OR)			
	B.	Explain high frequency & low frequency compensation.	IV	U	10
21.	**A.**	Explain digital color TV receiver with neat block diagram.	V	U	10
		(OR)			
	B.	Explain telecine equipment with neat block diagram.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 632 TEST ENGINEERING
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's level**
17.	Define Test engineering.	I	R
18.	Define Digital Guarding.	II	R
19.	Mention the Passive and Active Components.	III	U
20.	Expand BSDL.	IV	R
21.	Expand SVF.	IV	U
22.	Define Digital Simulator.	V	R
23.	Mention the characteristics of Passive and Active Components.	III	U
24.	Mention the application of Boundary Scan Test.	IV	U
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's level**
25.	Define passive and active components.	III	R
26.	Mention need and importance of Test Engineering	I	R
27.	Define auto compensation	II	R
28.	Explain Digital Integrated Circuits.	II	U
29.	Define Clock Termination.	II	R
30.	Mention the need of boundary scan Test technique.	IV	R
31.	Explain JTAG Port.	IV	U
32.	Explain Test Fixtures.	V	U

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's level**	**Max marks**
17.	**A.**	Explain the principles of fundamental Testing Methods and Memory Testing.	I	U	10
		(OR)			
	B.	Explain Manual and Automated PCB Trouble Shooting Techniques.	I	U	10
18	**A.**	Explain functional Testing of Digital, Analog and Mixed Integrated Circuit.	II	U	10
		(OR)			
	B.	Explain different types of Memory Module functional Test.	II	U	10
19.	**A.**	Explain Component Identification of Ageing Effects with VI Curve Trace.	III	U	10
		(OR)			
	B.	Explain Input and Output Characteristics of Digital Integrated Circuits.	III	U	10
20.	**A.**	Explain Principle of Boundary Scan Test and Boundary Scan Architecture with neat diagram.	IV	U	10
		(OR)			
	B.	Explain Digital Integrated Circuit Test using Boundary Scan Techniques.	IV	AP	10
21.	**A.**	Explain ATE in PCB Test.	V	AP	10
		(OR)			
	B.	Explain Standard Test Data Format.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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ECC 633 MOBILE COMMUNICATION
MODEL QUESTION PAPER

Time : 3 hrs **Max marks : 75**

PART-A (5x2=10Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's level**
1.	Define mobile communication.	I	U
2.	Define Paging system.	I	R
3.	Expand DVB.	II	U
4.	Expand CDMA.	III	R
5.	Expand UMTS.	III	U
6.	Expand GPRS.	IV	R
7.	Define WAP Gateway.	IV	AP
8.	Define Agent discovery	V	U
PART-B (5x3=15Marks)			
Answer any 5 Questions			
S.No		**Unit**	**Bloom's level**
9.	Explain channel assignment strategies.	I	U
10.	Define Cell splitting.	I	U
11.	Define Frequency reuse.	I	U
12.	Define cyclical repetition of data.	II	R
13.	Draw the frame structure for GSM.	III	U
14.	Define Radio subsystem.	III	AP
15.	Explain Quality of service in 3G.	IV	U
16.	Define Snooping	V	U

PART-C (5x10=50 Marks)					
Answer all Questions choosing either division (A) or division (B) of each question					
S. No			**Unit**	**Bloom's level**	**Max marks**
17.	**A.**	Explain Cordless telephones systems and Cellular telephone Systems.	I	U	10
		(OR)			
	B.	Explain Hand off Strategies, Prioritizing Handoffs, Interference and system capacity, in cellular systems.	I	U	10
18	**A.**	Explain Digital video broadcasting and Digital audio broadcasting.	II	U	10
		(OR)			
	B.	Explain Convergence of broadcasting and mobile communications.	II	U	10
19.	**A.**	Explain DECT system architecture with neat diagram.	III	U	10
		(OR)			
	B.	Explain CDMA digital cellular standard (IS – 95), Forward CDMA channel and Reverse CDMA channel.	III	U	10
20.	**A.**	Explain GPRS Functional groups and architecture with neat diagram.	IV	U	10
		(OR)			
	B.	Explain Paradigm Shifts in 3G Systems and Wireless OS for 3G handset.	IV	U	10
21.	**A.**	Explain Dynamic host configuration protocol and mobile ad-hoc network.	V	U	10
		(OR)			
	B.	Explain Destination sequence distance vector and Dynamic source routing.	V	U	10

Note: The question paper setters are requested to follow the Revised Bloom's Taxonomy levels as presented below:

Bloom's Taxonomy	Lower Order Thinking Skills (LOTs)	Higher Order Thinking Skills (HOTs)
Level	R-Remember, U-Understand , Ap-Apply	An-Analyze, E-Evaluate, C-Create
% to be included	90%	10%

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Department of Electronics and Communication Engineering
Equivalent Papers

BSCHEME		CSCHEME	
Subject Code	**Subject**	**Subject Code**	**Subject**
III Semester			
ECB 310	Electronic Devices and Circuits	ECC 310	Electronic devices and circuits
ECB 320	Electrical Circuits and Instrumentation	ECC 320	Electrical circuits and Instrumentation
ECB 330	'C' Programming	ECC 330	Programming in 'C'
ECB 340	Electronic Devices and Circuits Practical	ECC 340	Electronic Devices and Circuits Practical
ECB 350	Electrical Circuits and Instrumentation Practical	ECC 350	Electrical Circuits and Instrumentation Practical
ECB 360	'C' Programming Practical	ECC 360	"Programming in C" Practical
ECB 370	Computer Application Practical	ECC 370	Computer Application Practical For Electronics
IV Semester			
ECB 410	Industrial Electronics	ECC 410	Industrial Electronics
ECB 420	Communication Engineering	ECC 420	Communication Engineering
ECB 430	Digital Electronics	ECC 430	Digital Electronics
ECB 440	Linear Integrated Circuits	ECC 440	Linear Integrated Circuits
ECB 450	Industrial Electronics & Communication Engineering Practical	ECC 450	Industrial Electronics and Communication Practical
ECB 460	Integrated Circuits Practical	ECC 460	Integrated Circuits Practical
ECB 470	Communication and Life Skills Practical	ECC 470	Life and Employability Skill Practical

B-SCHEME		C-SCHEME	
Subject Code	**Subject**	**Subject Code**	**Subject**
V Semester			
ECB 510	Advanced Communication Systems	ECC 510	Advanced Communication Systems
ECB 520	Microcontroller	ECC 520	Microcontroller
ECB 530	Very Large Scale Integration	ECC 530	Very Large Scale Integration
ECB 541	**Elective – I** Digital Communication	ECC 541	**Elective I** Digital Communication
ECB 550	Advanced Communication Systems & Digital Signal Processing Practical	ECC 550	Advanced Communication Systems Practical
ECB 560	Microcontroller Practical	ECC 560	Microcontroller Practical
ECB 570	Very Large Scale Integration Practical	ECC 570	Very Large Scale Integration Practical
VI Semester			
ECB 610	Embedded Systems	ECC 610	Embedded Systems
ECB 620	Computer Hardware and Network	ECC 620	Computer Hardware Servicing And Networking
ECB 631	**Elective – II** Television Engineering	ECC 631	**Elective-II** Television Engineering
ECB 640	Embedded Systems Practical	ECC 640	Embedded Systems Practical
ECB 650	Computer Servicing and Network Practical	ECC 650	Computer Hardware Servicing And Networking Practical
ECB 660	Simulation Practical	ECC 660	Advanced Microcontroller And Simulation Practical
ECB 670	Project work	ECC 670	Project work